

## Build Fast VCAs and VCFs with Analog Multipliers

by Barrie Gilbert, Charles Kitchin and Ken Weigel

*By using a high-speed analog-multiplier IC, you can accomplish signal-processing tasks that are beyond the reach of current digital technology. One such chip allows you to design megahertz-range voltage-controlled amplifiers and filters.*

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If you understand the circuitry and operating principles of a high-speed, monolithic, dual-channel analog multiplier, you can realize useful signal-processing functions that are difficult or impossible to accomplish when using digital techniques. For example, you can design a variety of voltage-controlled-amplifier and filter circuits based on the 60-MHz (typ) AD539 analog multiplier, and by carefully choosing companion operational amplifiers for such circuits, you can exploit to best advantage the multiplier IC's speed and accuracy.

Because the multiplier's signal paths are almost transparent (ie, they introduce little signal delay or noise), you can use the IC to build voltage-tunable filters that operate at much higher frequencies than were formerly possible. These filters exhibit wide-range, stable  $Q$  factors and avoid the clock noise associated with switched-capacitor filters. As an example, you can use the multiplier to configure a 0.12%-linearity voltage-controlled filter with center frequencies as high as 100 kHz.

### A basic 2-quadrant multiplier

Before looking at specific applications for the multiplier, consider first how it performs its multiplication function. The AD539 has two signal inputs ( $V_{Y1}$  and  $V_{Y2}$ ), a common control input ( $V_X$ ), and a signal ground.

For the moment, however, treat the multiplier as if it had a single input,  $V_Y$  (Fig 1); the basic operation is the same for each multiplying channel of the device.

The common control input,  $V_X$ , controls a variable gain resistance,  $R_G$ , and the gain of the circuit is simply  $-R_Z/R_G$ . A fixed transresistance is formed by the op amp and  $R_Z$ , where  $R_Z$  is a feedback impedance built into the AD539. For  $V_X > 0$ ,

$$R_G = \frac{V_U}{V_W} \times R_Z,$$

where  $V_W$  is the output voltage and  $V_U$  is a propor-

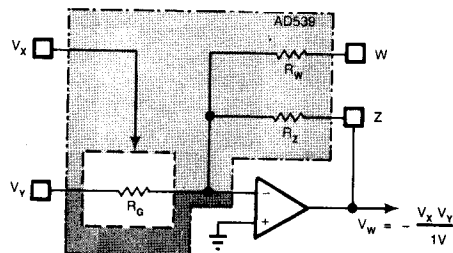


Fig 1—A basic 2-quadrant multiplier, in conjunction with an op amp, multiplies two input voltages  $V_X$  and  $V_Y$  to produce output voltage  $V_W$ .

## Multiplier design achieves high bandwidth and low distortion

tioning factor called the scaling voltage. The multiplier's transfer characteristic is

$$V_w = \frac{-V_x V_y}{V_u} \text{ for } V_x > 0.$$

When  $V_x$  is equal to or less than zero,  $R_G$  becomes an open circuit and the gain is zero. (The AD539 is designed in such a way that the operational amplifier in Fig 1 is external to the multiplier; thus, you can select from a wide range of available devices the op amp that best suits your application. You need one op amp for each channel of the multiplier.)

The multiplier IC is not quite as simple as Fig 1 shows, however. Input  $V_Y$  is buffered before it's applied to  $R_G$ , resulting in a constant input resistance of about 350 k $\Omega$ . The buffer has a limited signal range (specified as  $\pm 2V$  but usable to  $\pm 4V$  in many cases). Input  $V_x$  presents a relatively low input resistance of 500 $\Omega$ , and it has a full-scale range from zero to +3V with a 10% overrange capability. Values of  $V_x$  below zero will not cause signal feedthrough, but they could lead to control feedthrough in some applications.

The other resistance in the gain equation,  $R_Z$ , has a nominal value of 6 k $\Omega$ . To improve versatility, an identical resistor,  $R_w$ , halves the gain (ie, it doubles the

### The past and present of multipliers

Inexpensive monolithic multipliers first appeared around 1970, following the discovery of the translinear principle, which exploits the precise logarithmic properties of bipolar transistors. The first generation of such multipliers included simple diffused circuits of low accuracy (2 to 5% after manual trimming), and they required many external components.

As the art of multiplier design matured, it became possible to put the complete function—including input interfaces, output amplifier and scaling reference—on one chip, using stable thin-film resistors. With such devices, you could strap pins to perform multiplication and division and to calculate squares and square roots. It was still necessary, however, to compensate manually for three offset voltages and to calibrate the scale, an awkward and time-consuming chore. The limitations of the supporting circuitry prevented the full utilization of the inherently high bandwidth (about 50 MHz) of the multipliers' cores.

These limitations faded with the third generation of multipliers in the mid-1970s. These were individually calibrated by laser-trimming the thin-film resistors while the circuits were still in the wafer

stage. On-line instrumentation assured high accuracy by minimizing the total error of each device. The assembled circuit met the specified accuracy in all its basic configurations. However, the bandwidth was still only 1 MHz, and the distortion and noise performance were not outstanding.

The latest generation of multipliers addresses real-world signal-processing requirements more closely than its predecessors. Static accuracy—conformity to an ideal transfer characteristic under dc conditions—is now more than 100 times higher than that of early multipliers. More important, such neglected matters as bandwidth, differential gain and phase linearity and noise are now receiving more emphasis.

Today, analog multipliers are available in many types, differentiated by the actual function provided and the application. All have two input ports and one output port, and they all generate the product of the two inputs. An important class of these circuits accepts inputs of either polarity and preserves the signs to generate an output. When both inputs have essentially linear amplitude response the device is a 4-quadrant multiplier.

A second class of multiplier accepts a bipolar input at its linearly responding input port but responds to only one polarity at its control port. In this 2-quadrant device, only the signal input can change sign. The AD539 is a 2-quadrant multiplier: Its control input (X) can be positive only (0 to 3V full scale), whereas the signal inputs (Y) can be bipolar ( $\pm 2V$  full scale).

As is often the case, a tradeoff in performance in one area results in worthwhile improvements elsewhere. For example, in voltage-controlled amplifiers, it is unnecessary and undesirable for the multiplier to respond to both polarities at the control input because the primary objective is to control only the magnitude of the output, not its phase. Two-quadrant multipliers provide greater gain accuracy and lower noise than comparable 4-quadrant devices in such applications.

Finally, some applications—mostly in analog computing—require operation in only one quadrant. One-quadrant devices sometimes appear as log-antilog circuits and usually have high static accuracy at the expense of speed.

value of  $V_U$  to 2V) when placed in parallel with  $R_Z$ . This gain-adjustment capability is useful when you want to maintain the output swing at a value that's near the same level as the input.  $R_W$  can also be used to add an additional signal to the output.

The output from the AD539 is actually a current of nominally  $\pm 1$  mA ( $\pm 2.2$  mA peak), which can drive a grounded resistive load as high as  $500\Omega$  at the multiplier's full bandwidth, conservatively rated at 30 MHz min. Balance between the two channels of the chip is excellent: Using precision  $50\Omega$  loads, the gains track

within 0.025 dB, and phase matches within  $\pm 0.1^\circ$  from dc to 10 MHz.

The use of external op amps provides other design benefits. For instance, without external op amps, you must use low-resistance loads to profit from the full bandwidth of the AD539's signal channels, but such loads limit outputs to a few hundred millivolts. Also, the loading affects the scaling; it becomes less exact, because it involves the ratio of the external load to the internal thin-film resistors (which have an absolute tolerance of about 20%).

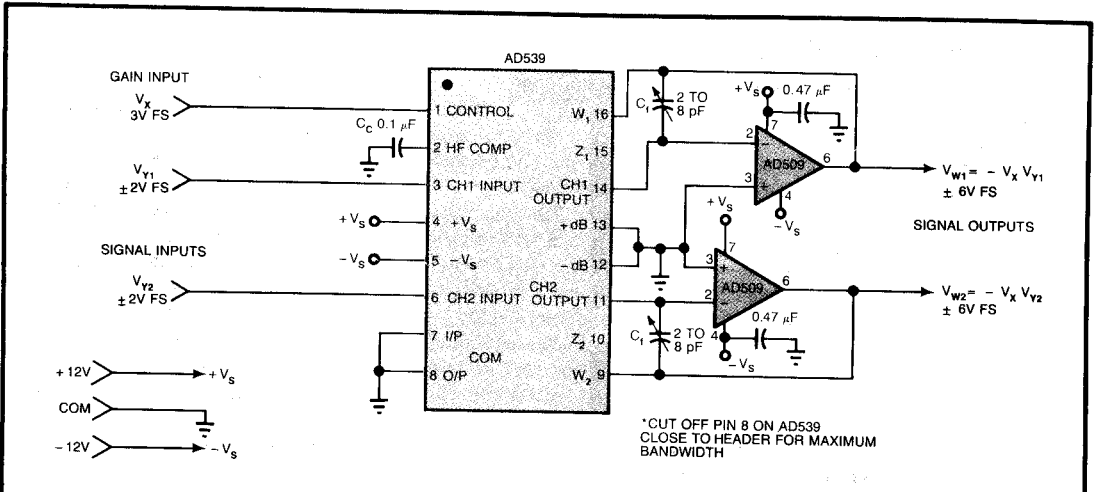


Fig 2—This dual-channel voltage-controlled amplifier (VCA) exhibits 0.05% total harmonic distortion at 10 kHz.

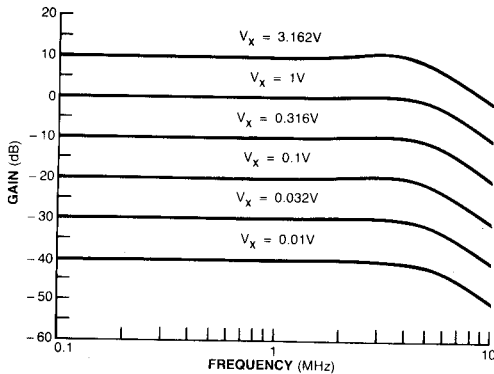


Fig 3—The frequency response of the Fig 2 dual-channel VCA incorporating an AD509 op amp demonstrates that signal bandwidth is virtually independent of gain.

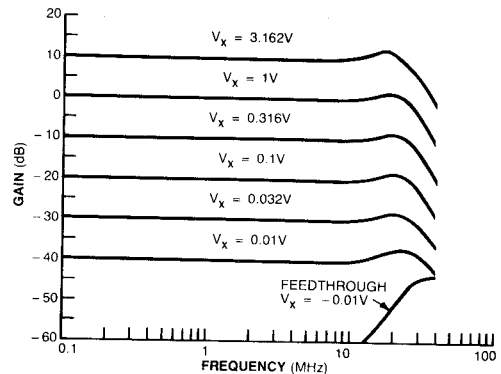


Fig 4—The -3dB bandwidth exceeds 25 MHz when you use the ADLH0032 hybrid op amp in the Fig 2 dual-channel VCA.

# Chip multiplies signal input by magnitude of control voltage

However, when you use external op amps and the IC's internal feedback resistors  $R_Z$  and  $R_W$  to provide current-to-voltage conversion, the ratio of these current-to-voltage conversion, the ratio of these matched internal resistors with respect to  $R_G$  determines the scaling and thereby guarantees high accuracy.

Furthermore, the performance of the op amp primarily determines the bandwidth capability of the circuit. For example, using an AD509 op amp, the -3-dB bandwidth is about 6 MHz; using an ADLH0032 hybrid op amp, 25 MHz is possible. And in situations

## Controlled-cascode design

The AD539 employs a controlled-cascode design that allows it to operate at frequencies to 60 MHz. In contrast, a typical 2-quadrant multiplier (Fig A) consists of a translinear cell ( $Q_1$  through  $Q_4$ ) and a voltage-to-current converter ( $Q_5$ ,  $Q_6$  and  $R_V$ ). Translinear circuits operate entirely in the current mode; their behavior is largely dependent on the ratios of currents, which result from the linear dependence of transconductance on current.

Input voltage  $V_Y$  determines the value of a pair of complementary currents through  $Q_1$  and  $Q_2$ . Because the ratio  $I_{Q3}/I_{Q4}$  is equal to  $I_{Q1}/I_{Q2}$  and the magnitude of the output is proportional to  $I_X$ , the overall circuit behaves as a controlled transresistance of value  $R_V I_Y / I_X$ .

There are several sources of distortion and noise in this circuit:

- $V_{BE}$  mismatch in  $Q_1$  through  $Q_4$  generates even-order distortion, the magnitude of which is independent of  $I_X$ .
- Junction resistance causes odd-order distortion, which is zero at only one  $I_X$  value.
- Junction resistances also generate a noise component proportional to  $I_X$ .
- Collector-base capacitances at  $Q_3$  and  $Q_4$  leak high-frequency signals to the output even when the dc gain is zero.

A controlled-cascode design addresses these problems by changing the location of the output (Fig B). Although the differential

signal current is still applied to  $Q_1$  and  $Q_2$ , the output is now taken from their collectors. When  $I_X=0$ ,  $Q_3$  and  $Q_4$  are off, and the circuit is simply a cascode circuit. There are no mechanisms for even- or odd-order distortion generation other than the negligible effect of nonlinear alpha. The base resistances no longer contribute noise. The effective transresistance is now simply  $R_V$ ; it does not depend on the accuracy of a current ratio as in the previous circuit.

When  $I_X$  is equal to  $I_Y$ , the source currents are completely diverted from  $Q_1$  and  $Q_2$ , so the output shuts off. The high-frequency feedthrough is now very small because  $C_{BC}$  of  $Q_1$  and  $Q_2$  no longer connect the input to the

output. For values of  $I_X$  between zero and  $I_Y$ , the effective transresistance is  $R_V / (1 - (I_X / I_Y))$ . Consequently, the circuit behaves like a cascode that has controllable gain. Analysis shows that the distortion caused by area mismatches and resistances is much lower than that of the first circuit.

The controlled cascode used in the AD539 is a derivative of Fig B's circuit. It's a configuration that also eliminates a troublesome peak in high-frequency response arising from  $C_{BC}$  of  $Q_3$  and  $Q_4$ . Furthermore, the design of the cell transistors achieves a balance between the conflicting requirements of low- and high-frequency accuracy.

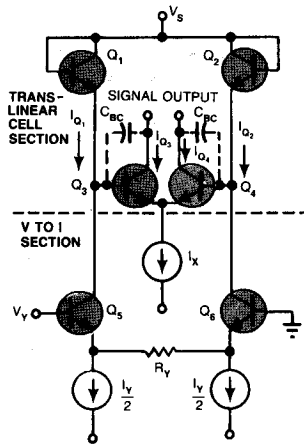


Fig A—A typical 2-quadrant multiplier cell has several sources of distortion and noise.

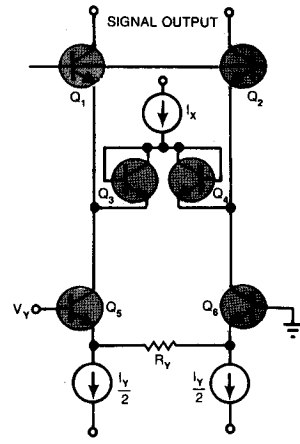


Fig B—The controlled-cascode multiplier cell minimizes distortion by furnishing a signal output at the collectors of  $Q_1$  and  $Q_2$ .

where bandwidth is not an issue, many low-cost op amps are sufficient. An AD611, for example, provides low distortion and a full  $\pm 10\text{V}$  output at frequencies as high as 200 kHz.

### Design a voltage-controlled amplifier

Fig 2 shows a dual-channel amplifier that has voltage-controllable gain. This gain is numerically equal to the control voltage  $V_X$  in the range 0 to +3.3V. The signal bandwidth is essentially independent of gain, as shown in Fig 3. In addition, the control-channel bandwidth is about 5 MHz (for a  $V_X$  rated from 300 mV to 3V), using a 3-nF HF compensation capacitor ( $C_C$ ). When rapid gain control is not required,  $C_C$  should be 0.1  $\mu\text{F}$ ; this value reduces high-frequency distortion in the signal channels. In addition, the  $\pm 12\text{V}$  supplies allow the circuit to realize a full-scale output swing of  $\pm 6\text{V}$  with some overrange. To avoid control breakthrough,  $V_X$  should not vary substantially from the nominal control range.

Looking at the performance of this voltage-controlled amplifier (VCA), the total harmonic distortion for an input of 1V rms is typically below 0.05% at 10 kHz, for a  $V_X$  above 300 mV. The output noise for a  $V_X$  of 1V is 50  $\mu\text{V}$  rms from 10 Hz to 10 kHz and 550  $\mu\text{V}$  from 10 Hz to 5 MHz. Furthermore, the signal leakage when  $V_X$  is deliberately made slightly negative (say, -10 mV) is -75 dB at 5 MHz.

If you need a higher bandwidth, you can use a hybrid op amp—for example, the ADLH0032. Fig 4 shows the

high-frequency response with  $C_F$  adjusted for 1 dB of peaking; under these conditions, the -3-dB bandwidth exceeds 25 MHz. Careful board layout and supply decoupling keep signal leakage below -90 dB at low frequencies and below -60 dB at 20 MHz when  $V_X$  is -10 mV.

To meet more stringent design requirements, you can employ an ultralow-distortion single-channel VCA (Fig 5). In this design, the input connects directly to channel 1 and to amplifier  $A_1$ . This amplifier inverts the

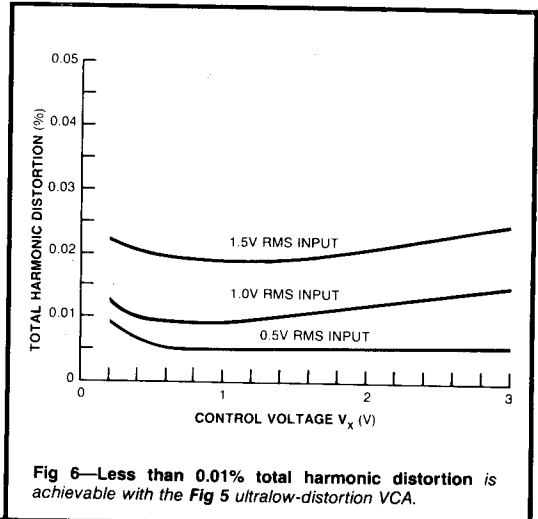


Fig 6—Less than 0.01% total harmonic distortion is achievable with the Fig 5 ultralow-distortion VCA.

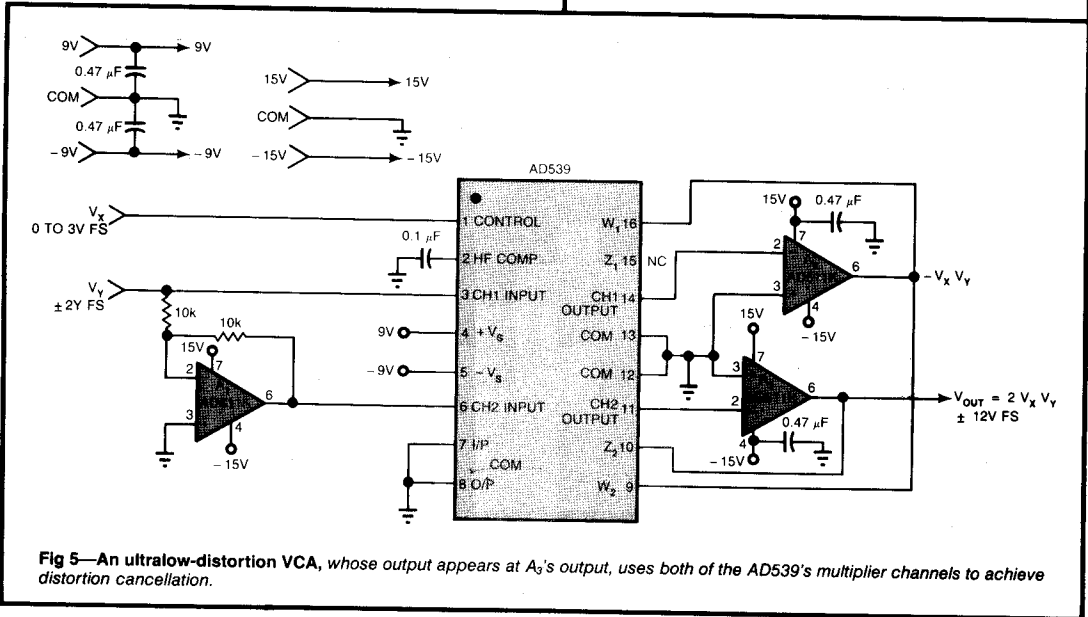


Fig 5—An ultralow-distortion VCA, whose output appears at  $A_2$ 's output, uses both of the AD539's multiplier channels to achieve distortion cancellation.

## Selection of external op amp determines circuit bandwidth

signal and drives the AD539's channel 2. Driving the multiplier in symmetrical fashion minimizes distortion.

Note that this circuit provides two outputs. The output of channel 1's amplifier,  $A_2$ , is  $-V_X V_Y$ ; it can be used directly and has the same characteristics as the Fig 2 VCA. This output is also used to obtain the low-distortion  $A_3$  output, which is equal to  $2V_X V_Y$ .

For the low-distortion output,  $A_2$ 's output connects to one of channel 2's scaling resistors,  $W_2$ ; the other channel 2 scaling resistor,  $Z_2$ , provides the feedback path for channel 2's output amplifier,  $A_3$ . Because these internal resistors are matched,  $A_3$  simply inverts the output of  $A_2$ . At the same time, it performs current-to-voltage conversion for channel 2 of the multiplier and adds the result to the inverted  $A_2$  output. Therefore, the total output of  $A_3$  is  $-(-V_X V_Y)$  from channel 1 and  $A_2$  plus  $-(-V_X V_Y)$  from  $A_1$  and channel 2; this amounts to  $2V_X V_Y$ . Amplitude limits on this low-distortion output arise from the supply voltages of  $A_2$  and  $A_3$ .

Fig 6 shows that the total harmonic distortion can remain below 0.01% over a wide gain range. The increase in distortion for small values of  $V_X$  apparently stems from noise in the measurement system. The balanced configuration of this VCA eliminates control feedthrough when  $V_X$  is outside its nominal range.

Many variations of this design are possible, with gains as high as 60 dB. What's more, a series connection

of the two channels creates a circuit that has a square-law gain response. This function is useful, for example, in swept-gain applications; it compensates for inverse-square-law propagation-path losses.

Two-quadrant multipliers also find profitable application in the construction of voltage-tunable filters. In such a design, a loop consisting of two integrators and

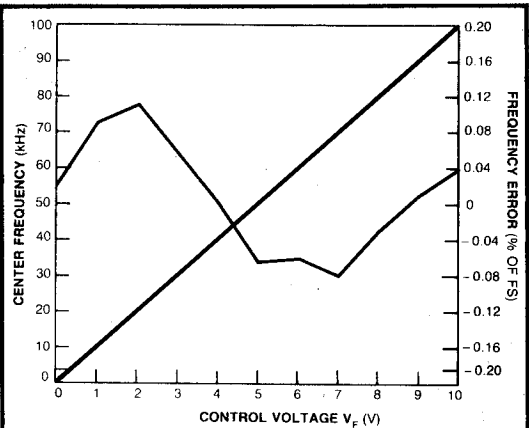


Fig 8—In response to a 0 to 10V control-voltage input, the Fig 7 voltage-tunable filter exhibits a 0- to 100-kHz center frequency. Frequency error remains less than 0.12%.

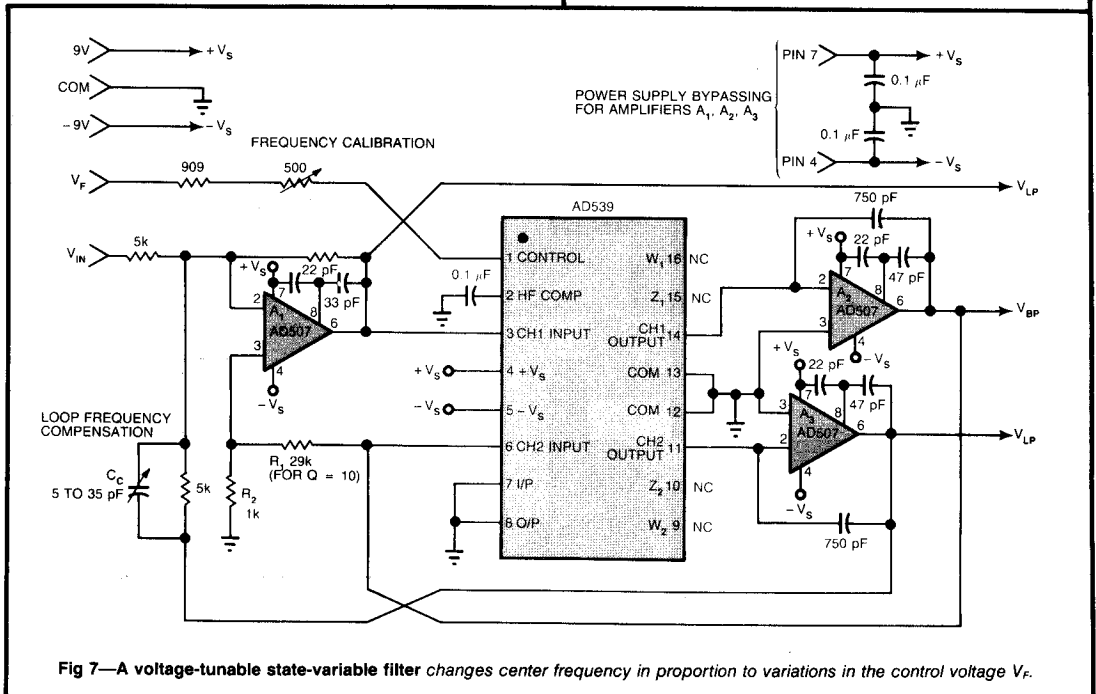


Fig 7—A voltage-tunable state-variable filter changes center frequency in proportion to variations in the control voltage  $V_F$ .



an inverter (used also as a summing amplifier) forms the basic filter. The filter has lowpass, highpass and bandpass responses, and it features a variable  $Q$  over a wide range. Furthermore, the low offset voltage of the control channel ensures accuracy over a much wider range of control voltages than is possible using a typical 4-quadrant multiplier.

In the integrators, pairs of capacitors and resistors determine the resonant frequency. To control this frequency, it's customary to vary the values of the resistors. Because the channels of an AD539 behave like voltage-controlled resistances, they allow you to create voltage-tunable filters.

A 2-pole voltage-tunable filter section (Fig 7) provides a center frequency of nominally 0 to 100 kHz, easily scaled to other ranges by the choice of capacitors (which should, however, always be equal). Each channel of the AD539 behaves like a voltage-controlled transresistance, having a value of

$$R_G = \frac{6 \text{ k}\Omega}{V_x / 1V}$$

The absolute value of  $R_G$  is not exact; only the ratios

of the on-chip resistors undergo trimming during manufacturing. Accurate, temperature-stable calibration of the frequency requires the addition of an external trim resistor, placed in series with the (resistive) control input. When the circuit is thus adjusted to compensate for the tolerance of the thin-film resistors, the resonant frequency is  $f = 10 \times V_F / 1V$  ( $f$  is in kilohertz,  $V_F$  in volts).

Fig 8 shows the measured center frequency of the voltage-tunable filter and the deviation from the ideal value. The deviation is less than 0.12% of the full range. With the values shown for  $R_1$  and  $R_2$ , the nominal  $Q$  is 10, and it varies by only a few percent over the 1- to 100-kHz range. In general,

$$Q = \frac{R_1 + R_2}{3R_2}$$

The minimum  $Q$ , 0.33, occurs when the value of  $R_2$  approaches infinity; the maximum  $Q$  is limited in practice by dynamic-range considerations. Capacitor  $C_C$  helps to maintain loop stability and is adjusted for minimum variation of  $Q$  with  $V_F$ . If a higher bandwidth is necessary, high-speed op amps make feasible a

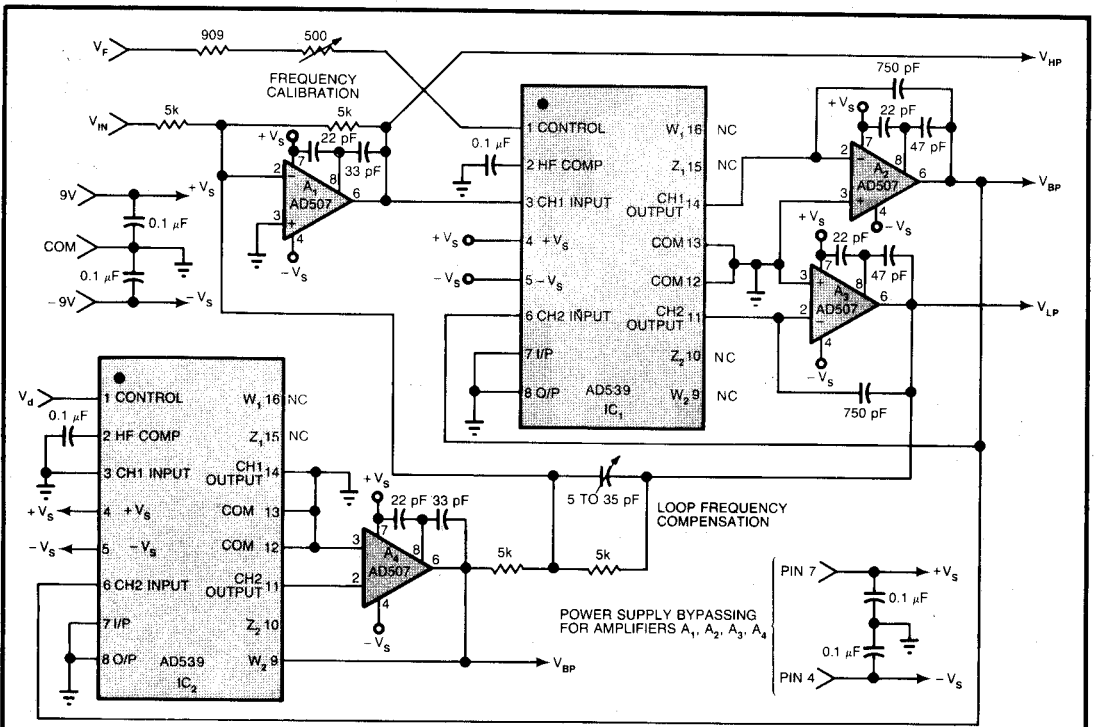


Fig 9—This variable- $Q$  voltage-tunable filter uses one multiplier to vary center frequency in response to  $V_F$  and a second one to vary the  $Q$  in response to changes in  $V_G$ .

## Distortion for 1V rms input is typically below 0.05% at 10 kHz

full-scale frequency of 1 MHz.

In any case, there are limits to the input amplitude. Note that the output of  $A_2$  is  $Q$  times larger than  $V_{IN}$ . This output drives the channel 2 input of the AD539, whose signal capacity is about  $\pm 4V$ . Consequently,  $V_{IN}$  must be less than  $\pm 4V/Q$  to avoid clipping.

A more sophisticated voltage-tunable filter provides voltage control of  $Q$ . The Fig 9 circuit incorporates two AD539s, one of which provides this function. The frequency scaling remains 10 kHz/V of  $V_F$ , but the damping ( $d$ ) is now equal to the numerical value of the control voltage,  $V_d$ . Consequently,

$$d = V_d, \quad Q = \frac{1}{V_d} (V_d \text{ in volts}).$$

If you need to alter the scaling of  $Q$ , connect a resistor in series with pin 1 of  $IC_2$ . You can use the bandpass output from the output of either  $A_2$  (in which case the gain is equal to  $Q$ ) or  $A_1$ . This second connection has the advantage of providing a gain that doesn't vary with the value of  $Q$ .

For the Fig 9 filter design, Fig 10 shows the ac output for  $V_d$  values of 100 mV, 300 mV, 1V and 3V (for  $Q=10, 3.3, 1$  and  $0.33$ , respectively). In addition, Fig 11 shows the stability of  $Q$  as  $V_F$  varies over its nominal range. Here,  $Q=10$  and  $V_F=100$  mV, 300 mV, 1V, 3V and 10V (for  $f=1, 3, 10, 30$  and  $100$  kHz, respectively).

Op-amp offset voltages can be troublesome for small values of  $V_F$ , when the dc behavior tends toward open-loop conditions. In applications requiring a wide range of frequency control, it's necessary to trim the offset voltages of amplifiers  $A_1$  through  $A_3$ .

In addition, compensation capacitors for the op amps must provide a safe stability margin without adding too much phase to the integrators. Such very fast op amps as the ADLH0032 require more complex high-frequency compensation, but filters designed for the audio range can use such inexpensive, internally compensated op amps as the AD611. Nominally, the frequency-compensation capacitor at pin 2 of the AD539 should be  $0.1 \mu F$ .

The output of the voltage supplies in these circuits is somewhat flexible. Figs 7 and 9 show 9V supplies for

the AD539s and the AD507s. In these applications, there is no advantage in using higher voltages. You can, however, use 15V supplies.

Finally, digital control of the center frequency or  $Q$  or both requires only the addition of a D/A converter. The AD558 is a good choice for this application, having a 2.5V full-scale output. Moreover, it's capable of using the same power supplies.

The AD539-based filter design stacks up favorably against a typical switched-capacitor filter (table). In comparison, the state-variable filter shown in Fig 7 exhibits 30 times the maximum center frequency, 25 times the dynamic range and five times the maximum  $Q$  at 20 kHz. The obvious tradeoff between these approaches is in current consumption: The AD539-based

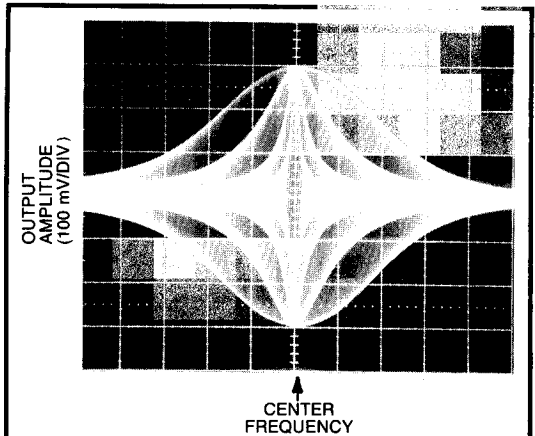


Fig 10—The wide variation of  $Q$  apparent in these superimposed outputs of the Fig 9 circuit stems from  $V_d$  values equaling 100 mV, 300 mV, 1V and 3V.

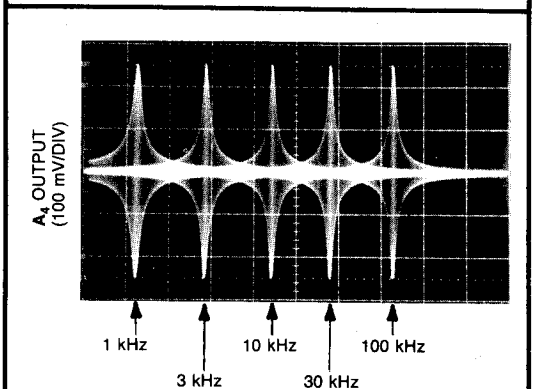


Fig 11—The stability of  $Q$  as  $V_F$  varies is illustrated by the uniform shapes of the Fig 9 circuit's ac response.

TABLE—COMPARISON OF AD539-BASED FILTER WITH TYPICAL SWITCHED-CAPACITOR FILTER

PARAMETER	SWITCHED-CAPACITOR FILTER	AD539 ANALOG FILTER
MAXIMUM $Q$ AT 20 kHz	10	50
MAXIMUM CENTER FREQUENCY	30 kHz	1 MHz
SIGNAL DYNAMIC RANGE	52 dB	80 dB
POWER-SUPPLY CURRENT	4 mA	28 mA



## Distortion cancellation gives 0.01% total harmonic distortion

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filter consumes seven times the current. Nevertheless, the simplicity, accuracy and high bandwidth of the circuits using the AD539 can outweigh this disadvantage in most applications.

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