EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

AD7091R Evaluation Board (EVAL-AD7091RSDZ)
System Demonstration Platform (EVAL-SDP-CB1Z)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 is an ultralow, power data acquisition system using the AD7091R 12-bit, 1 MSPS SAR ADC and an AD8031 op amp driver with a total circuit power dissipation of less than 5 mW on a single 3 V supply.

The low power consumption and small package size of the selected components makes this combination an industry-leading solution for portable battery-operated systems where power dissipation, cost, and size play a critical role.

The AD7091R requires typically only 350 µA of supply current on the V_{DD} pin at 3 V, which is significantly lower than any competitive ADC offering currently available in the market. This translates to ~1 mW typical power dissipation.

The AD8031 requires only 800 µA of supply current, that results in 2.4 mW typical power dissipation at 3 V supply, making the total power dissipation of the system less than 5 mW when sampling at 1 MSPS with a 10 kHz analog input signal.

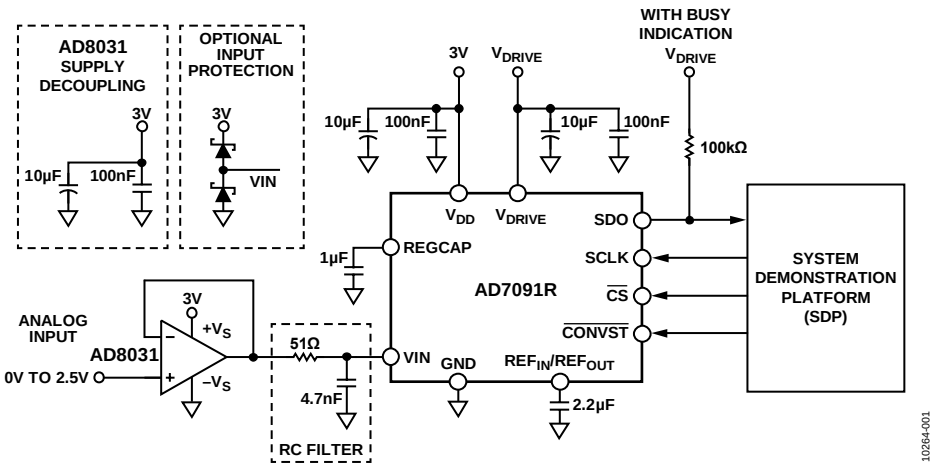

Figure 1. 12-Bit, 1 MSPS Low Power ADC with Driver (Simplified Schematic: All Connections Not Shown)

CIRCUIT DESCRIPTION

To maximize performance, most SAR ADCs require a suitable input buffer for the analog signal. The buffer isolates the source from the transients generated on the ADC input when the internal track-and-hold switch goes from hold to track. The buffer driving the ADC must recover from this transient and settle to the required accuracy within the acquisition time of the ADC. This is particularly important in applications where the signal source has high source impedance and where low distortion and a high signal-to-noise ratio is important. Selecting the proper buffer op amp is therefore a critical part of the design process.

The AD7091R is a 12-bit, fast, ultralow power, single-supply ADC with an internal 2.5 V reference. The part can be operated from a 2.7 V to 5.25 V supply. The AD7091R is capable of throughput rates of 1 MSPS. At a sampling rate of 1 MSPS, the total power dissipation of the AD7091R with a 10 kHz input signal is approximately 2.3 mW.

This power figure can be reduced in applications where 1 MSPS sampling frequency is not necessary because the AD7091R power scales with the throughput, as shown in Table 1.

To further reduce power dissipation of the system, reduce the throughput rate of the converter. Table 1 shows the typical power vs. throughput for the AD7091R at 3 V when operating in normal mode.

Table 1 shows the reduction in power consumption that is achievable when power-down mode is activated. The power-down mode is an extremely useful method to significantly reduce power supply requirements when operating the AD7091R at lower throughput rates.

The AD7091R is housed in a tiny, 3 mm × 2 mm, 10-lead LFCSP or a 3 mm × 5 mm, 10-lead MSOP. Both packages offer considerable space saving advantages over competitive solutions.

The AD8031 is a rail-to-rail input/output low power operational amplifier and is an optimum drive amplifier for the AD7091R. The AD8031 can operate from a 2.7 V to 12 V supply, which allows both ICs to be driven from the same supply rail. The AD8031 has an 80 MHz bandwidth, a 30 V/µs slew rate, and a 125 ns settling time to 0.1%.

When operating on a single supply, the output of the AD8031 can go to within 20 mV of the negative rail. If linearity to 0 V input is needed, the AD8031 requires an additional negative supply (see Tutorial MT-035).

Figure 1 shows the simplified schematic for the circuit. Well decouple the IC power supply pins to ground using 100 nF and 10 µF ceramic capacitors. Position these capacitors as close as possible to the supply pins of both ICs.

Take care to ensure that the analog input signal to the ADC does not exceed the supply rails by more than 300 mV. If the signal does exceed this level, the internal ESD protection diodes become forward-biased and start conducting current into the substrate. A diode can conduct a maximum current of 10 mA without causing irreversible damage to the part. This can be prevented by connecting a pair of Schottky diodes between VIN and the supply rails of the AD7091R, as described in Tutorial MT-036).

The AD7091R contains an internal 2.5 V reference. Well decouple the REF_{IN}/REF_{OUT} pin to achieve the specified performance. The typical value for the REF_{IN}/REF_{OUT} capacitor is 2.2 µF. Note that the internal reference voltage can be overdriven externally.

If an external reference voltage is used, the range must be between 2.7 V to V_{DD}, and it must be connected to the REF_{IN}/REF_{OUT} pin. A typical value for the regulator bypass (REGCAP) decoupling capacitor is 1 µF.

The voltage applied to the V_{DRIVE} input controls the logic level voltage of the serial interface. Connect this pin to the supply voltage of the logic family connected to the AD7091R digital outputs. V_{DRIVE} can be set in the 1.8 V to V_{DD} range. Typical values for the V_{DRIVE} decoupling capacitors are 100 nF in parallel with 10 µF.

If the busy indication function is required, connect a pull-up resistor of 100 kΩ between the V_{DRIVE} and the SDO pin.

The AD8031that is used to buffer analog input of the AD7091R is configured as a unity gain buffer. A single-pole RC filter follows the op amp output stage to reduce out-of-band noise. The cutoff frequency of the RC filter is set to 660 kHz. However, depending on the system throughput rate specification, this parameter can vary. In systems where the AD7091R is not operated at maximum throughput rate, the filter cutoff frequency can be reduced. Depending on the analog signal input amplitude and offset, the AD8031 operational amplifier can be configured to provide gain, attenuation, and level shifting, to match the input signal swing to the analog input range of the ADC.

Table 1. Typical Power vs. Throughput for the AD7091R at 3 V when Operating in Normal Mode

Mode	I_{DD}	I_{DRIVE}	I_{AMP} (µA)	Total Current (µA)	Total Power (mW)
Power Down	550 nA	36 nA	766	767	2.3
Static (Power On, Input Grounded, No Clock)	21 µA	81 nA	766	787	2.4
Operating (Power On, 10 kHz Input, 1 MSPS Sampling)	368 µA	406 µA	766	1540	4.6
Operating (Power On, Input Grounded, 1 MSPS Sampling)	344 µA	35 µA	766	1145	3.4
Operating (Power On, Input Grounded, 1 kSPS Sampling)	57.8 µA	18.9 µA	766	843	2.5

Note that convert start pulse width = 20 ns when sampling, $V_{DD} = V_{DRIVE} = 3$ V.

Figure 2 and Figure 3 show the integral nonlinearity (INL) and differential nonlinearity (DNL) plots for the circuit. Note that the INL and DNL is less than ±1 LSB.

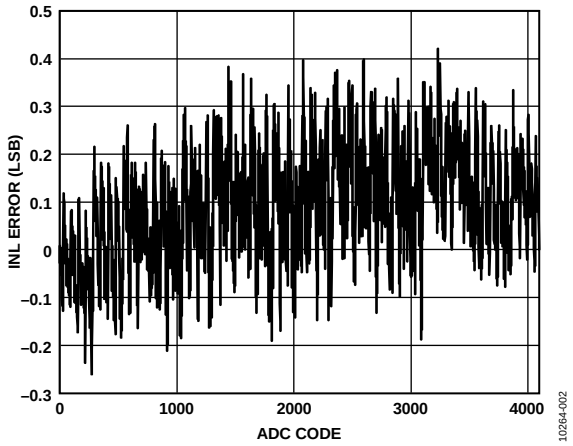

Figure 2. INL for Sampling Rate of 1 MSPS

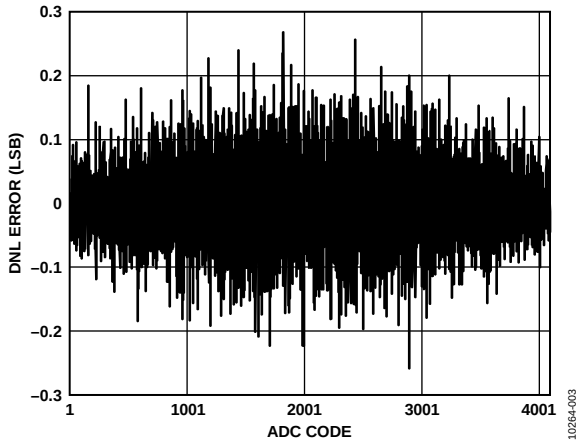

Figure 3. DNL for Sampling Rate of 1 MSPS

Figure 4 displays the FFT data calculated for 8192 samples captured at the 1 MSPS rate with an analog input frequency of 10 kHz. The SNR is 70.44 dBFS.

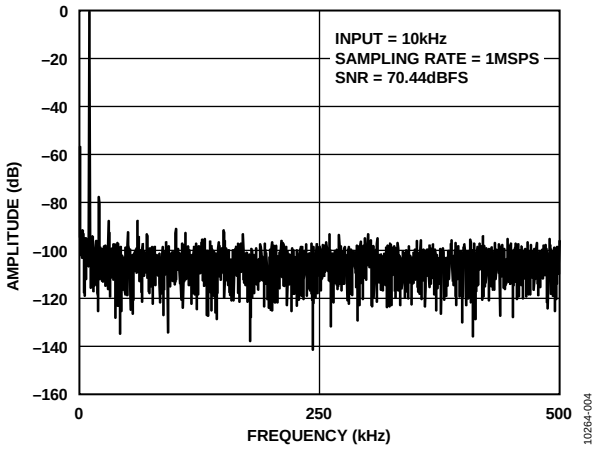

Figure 4. FFT of System, Input =10 kHz, Sampling Frequency = 1 MSPS

The circuit must be constructed on a multilayer printed circuit board (PCB) with a large area ground plane. Proper layout, grounding, and decoupling techniques must be used to achieve optimum performance (see Tutorial MT-031, Tutorial MT-101, and the AD7091R evaluation board layout shown in the CN-0247 Design Support Package.

Values of the components surrounding the AD7091R and the AD8031 can be modified to meet specific requirements of the application and sensor. For example, the buffer can be configured to provide gain and offset, and the cutoff frequency of the RC filter can be changed depending on the sampling frequency and input frequency.

A complete documentation package including schematics, board layout, and bill of materials (BOM) can be found at http://www.analog.com/CN0247-DesignSupport.

COMMON VARIATIONS

The AD7091 is similar to the AD7091R and is available in an 8-lead 2 mm × 2 mm LFCSP. The AD7091 uses the V_{DD} supply as a reference and does not contain an internal one.

CIRCUIT EVALUATION AND TEST

The EVAL-AD7091RSDZ evaluation board is developed to evaluate and test the AD7091R device with the circuitry described in this circuit note. A detailed schematic and user instructions are available in the EVAL-AD7091RSDZ documentation. A functional block diagram of the test setup is shown in Figure 5.

Equipment Needed

The following equipment is required to test the circuit:

- EVAL-AD7091RSDZ Evaluation Board (includes software and 9 V dc wall wart power supply)
- EVAL-SDP-CB1Z System Demonstration Platform Board
- A low distortion signal generator, such as the Agilent 81150A or Audio Precision System Two 2322
- A PC with an USB 2.0 Port running Windows® XP, Windows Vista, or Windows 7 (32-Bit or 64-bit)
- Power supplies: 9 V dc wall wart (included with evaluation board, external 3 V dc supply at 50 mA)

Setup

Before connecting any hardware, ensure that the links on the EVAL-AD7091RSDZ evaluation board are positioned as follows:

- LK1: Position A (selects the AD8031 as the input buffer)
- LK2: Position A (connects the input at J5 to the input buffer)
- LK5: Position A (enables external V_{DRIVE} source)
- LK6: Position B (enables external V_{DD} source)

From this point, follow the evaluation board documentation to connect the hardware and install the software.

Test

Refer to the evaluation board documentation for the complete description on how to run the various tests contained in this circuit note.

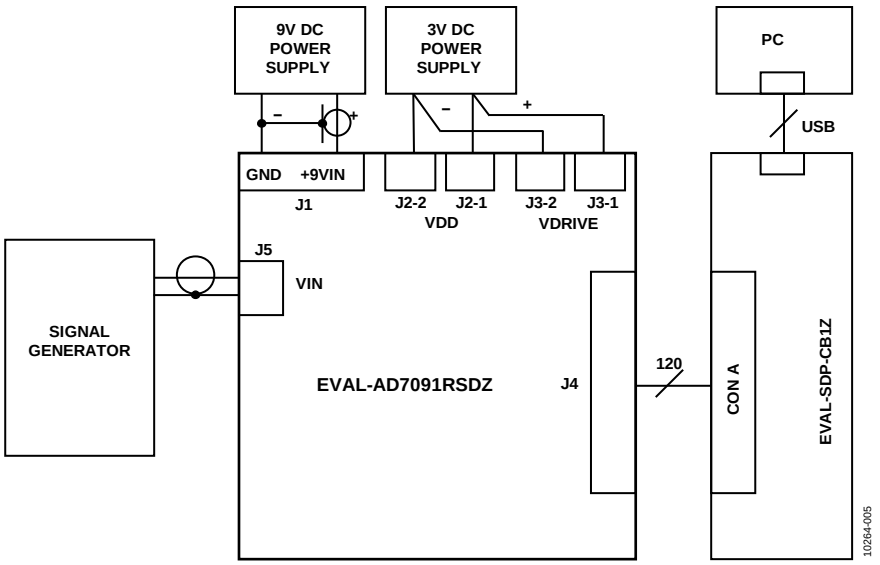

Figure 5. Functional Diagram of Test Setup

LEARN MORE

CN-0247 Design Support Package:
http://www.analog.com/CN0247-DesignSupport

MT-031 *Tutorial, Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*, Analog Devices.

MT-035 Tutorial, *Op Amp Inputs, Outputs, Single-Supply, and Rail-to-Rail Issues*, Analog Devices.

MT-036 Tutorial, *Op Amp Output Phase-Reversal and Input Over-Voltage Protection*, Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

Data Sheets and Evaluation Boards

AD7091R data sheet and evaluation board

System Demonstration Platform (EVAL-SDP-CB1Z)

AD8031 Data Sheet

REVISION HISTORY

4/12—Revision 0: Initial Version

CN10264-0-4/12(0)