AN-5015

Fairchild Semiconductor
Application Note
December 1999
Revised December 2000

FAIRCHILD SEMICONDUCTOR™

USB1T11A Transceiver and Specification Compliance

Introduction

The Universal Serial Bus (USB) specification has become widely accepted as the preferred mechanism for low to medium speed serial data interfaces. Older connections like RS232 and parallel printer LPTx ports can only be connected to one device at a time. USB allows multiple devices to be attached to a single port enabling greater system flexibility. The USB specification also allows for the connection, immediate operation, and removal of these devices with the system running. With widespread use comes the need to develop low cost, specification compatible, interface devices. An USB implementation example is shown in Figure 1.

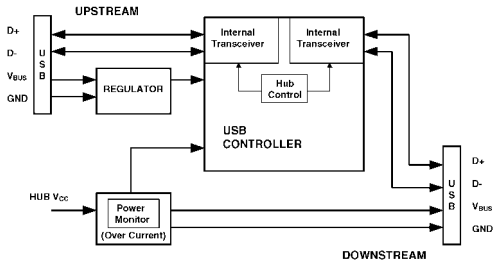


FIGURE 1. USB with Integrated Transceiver

Benefits of Standalone Transceiver

Removing the transceiver function from the Digital Controller and Serial Interface Engine (SIE) has three main benefits.

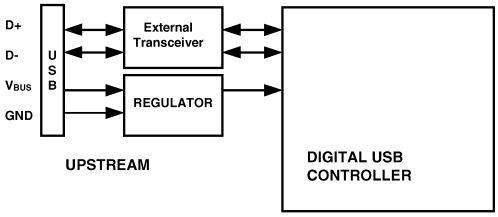


FIGURE 2. USB with Standalone Transceiver

1. Removes signal integrity concerns from the digital controller. The standalone USB Transceiver is responsible for meeting all compliance and signal quality issues related to driving and receiving differential signals on the USB cable.
2. Isolates the digital controller from the cable. Guaranteed ESD tolerance on the transceiver ensures the expensive controller will not be damaged by adverse signals on the cable.
3. Removes analog style signals from the digital controller. This allows the design of the digital controller to be optimized for USB logic functionality. Keeping the controller completely digital reduces the design “risk” and added cost of a mixed analog and digital design.

Transceiver Block Diagram and Pinout

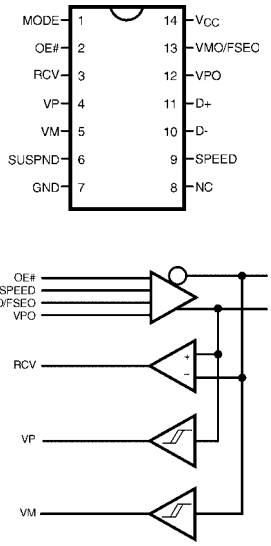


FIGURE 3. Functional Diagram and Pinout

Transceiver Features

1. Converts USB differential voltages to digital logic signal levels.
2. Converts the D+ and the D– line to single ended logic outputs for SE0 (single-ended 0) detection.
3. Converts logic levels to different USB signals.
   - Runs at low or high speed
   - Selectable output slope control
   - Meets the USB 1.1 drive template
   - Has low power standby mode
4. Small footprint at low cost.

Backwards Compatibility to USB 1.0

The USB Revision 1.0 and USB Revision 1.1 have many subtle differences. The differences however minor do serve to reduce the ambiguity of the 1.0 specification. The Fairchild USB1T11A has been designed to be compliant with USB 1.1 and backwards compliant to revision 1.0 of the USB standard.

USB 1.1 SYSTEM LEVEL GOALS

1. Provide hooks to make system software work better with both 1.0 and 1.1 Hardware.
2. Remove non-relevant information from the specification.
3. Remove redundant information.
4. Provide better definition and use of common terms in the specification.
5. Enhance the capabilities of USB in Revision 1.1.

USB 1.1 ELECTRICAL GOALS

1. Better define electrical tests and testing methodologies.
2. Clarify connection events.
3. Specify realistic loads for Low Speed Operation.

Breaking the electrical goals down to specific input and output specifications shows the similarities between the two USB specifications. The common mode input voltage for the differential receiver has been reduced from 0.8V – 2.5V to 0.8V to 2.3V. In addition, a crossover voltage range has been established for the differential outputs to maximize the reliability to USB signal transmission (see Figure 4). In order to be backward compatible with USB 1.0, the Fairchild USB1T11A specifies a common mode input range of 0.8 to 2.5 volts.

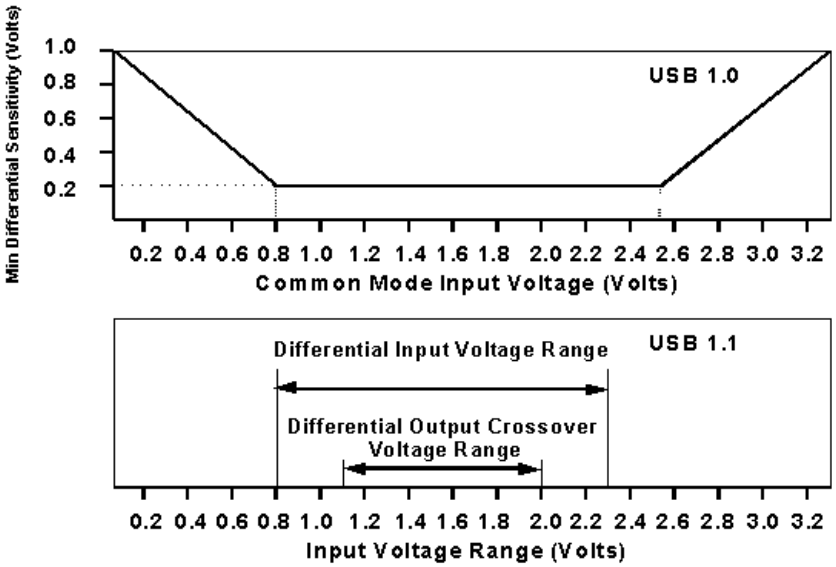


FIGURE 4. USB Common Mode Voltage for Differential Receiver

Backwards Compatibility to USB 1.0 (Continued)

The differential output impedance of the CMOS buffers has been updated to include the series termination resistance. The USB 1.0 specification required buffer impedance from 3 – 15Ω and a series resistance of 27Ω to produce equivalent output impedance ranging from 30Ω to 42Ω. The USB 1.1 specification only requires the combined output buffer impedance and series resistance to fall within a range from 28Ω to 44Ω. Devices compliant to version 1.1 of the specification will recommend the value of series resistance to meet this specification. The reverse is also true, devices compatible to 1.1 are backward compatible to revision 1.0 if they can produce equivalent output impedance which meets the tighter 1.0 specification. See the output impedance equation and Figure 5 for the Fairchild USB1T11A transceiver.

Specified Output Impedance: 6–18Ω

Recommended Series Resistance: 24Ω

Lowest Equivalent Output Impedance = 6Ω + 24Ω = 30Ω

Highest Equivalent Output Impedance = 18Ω + 24Ω = 42Ω

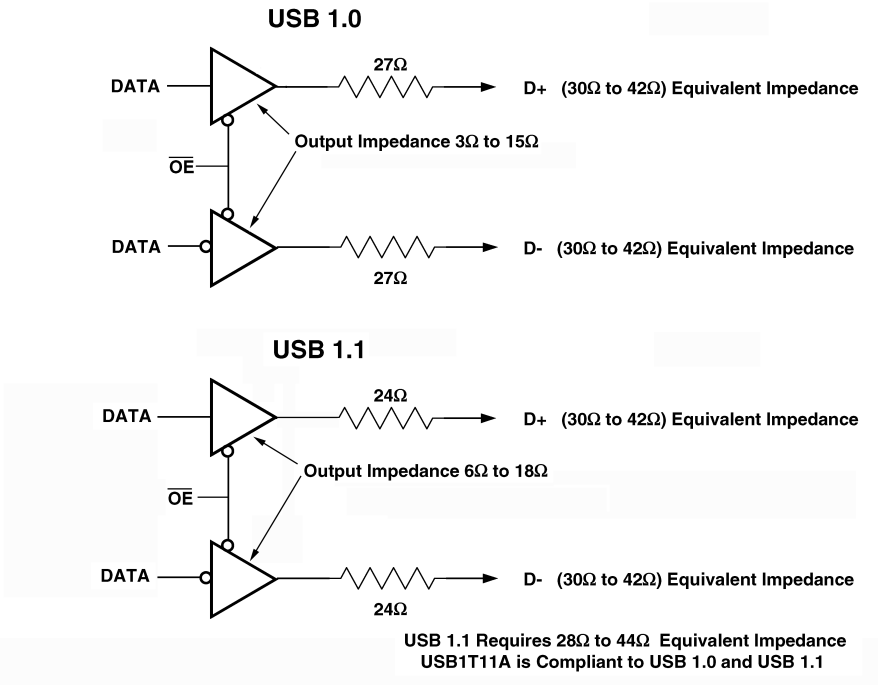


FIGURE 5. Output Impedance Compliance to USB Specifications

Transceiver Compliance to USB 1.1

The following table has been extracted from USB Compliance Checklist version 1.05. Only checklist items relevant to the design and implementation of the USB transceiver are addressed in this document. In order to guarantee physical layer compliance, all relevant specifications are 100% production tested on the Fairchild USB1T11A and guaranteed in the datasheet.

TABLE 1. USB Compliance Specifications

ID	Question	Datasheet Specification
ST1	Is the data line crossover voltage between 1.3 and 2.0V?	V_{CR}: 1.3V – 2.0V
ST2	Do all single ended receivers recognize 0.8V or below as a logic low?	V_{SE}: 0.8V (Logic Low)
ST3	Do all single ended receivers recognize 2.0V or more as a logic high?	V_{SE}: 2.0V (Logic High)
ST4	Do all differential receivers have an input sensitivity of at least 200 mV between 0.8 and 2.5 volts common mode?	V_{DI}: 200 mV (min)
ST6	Is the input impedance of D+ and D–, without termination and pull up resistors, more than 300kΩ?	I_{OZ}: 10 µA (max)
LS1	Are data line rise times between 75 ns and 300 ns when driving into any single ended, capacitive load between 200 and 450 pF?	t_{LR}: 75 ns – 300 ns
LS2	Are data line fall times between 75 ns and 300 ns when driving into any single ended, capacitive load between 200 and 450 pF?	t_{LF}: 75 ns – 300 ns
LS3	Are the rise and fall times matched to within 20% for J ≥ K transitions?	t_{REM}: 80 – 120% (slow)
LS4	Are the rise and fall times matched to within 20% for K ≥ J transitions?	t_{REM}: 80 – 120% (slow)
FS1	With series termination resistors, does the device's source impedance remain within the bounds of Figure 8 and Figure 9?	Z_{DRV}: 6 – 18Ω
FS2	Are data line rise times between 4.0 and 20 ns when driving into a single ended 50 pF load?	t_R: 4 ns – 20 ns
FS3	Are data line fall times between 4.0 and 20 ns when driving into a single ended 50pF load?	t_F: 4 ns – 20 ns
FS4	Are the rise and fall times matched to within 10% for J ≥ K transitions?	t_{RFM}: 90 – 110% (full)
FS5	Are the rise and fall times matched to within 10% for K ≥ J transitions?	t_{RFM}: 90 – 110% (full)

For a complete listing of the Fairchild USB1T11A features and specifications please follow the link to the datasheet below:

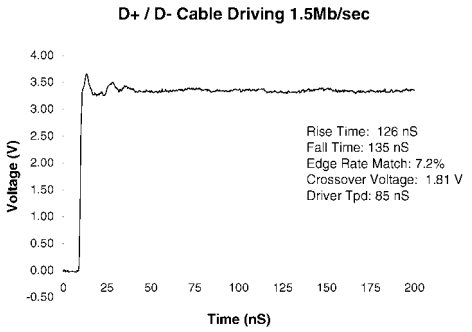
http://www.fairchildsemi.com/pf/US/USB1T11A.html#Datasheet

Transceiver Compliance in Suspend Mode

When directed by the digital controller, the USB1T11A transceiver will enter a suspend mode. In order to minimize device power consumption during suspend, the differential receiver must be shut down. In order to detect an end to USB suspend, the digital controller must monitor the state of VP and VM which remain active during the suspend state.

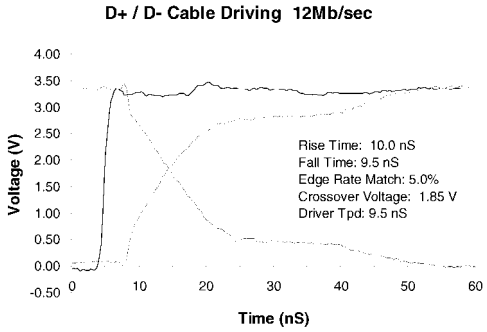
Transceiver Performance

Actual performance of the Fairchild USB Transceiver is outlined in the following graphs and waveforms.



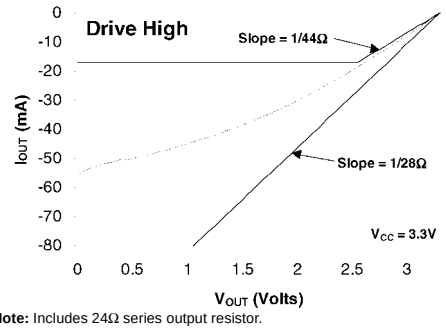
Note: In low speed testing, the downstream port included an additional 50 pf of load capacitance. Total C_{LOAD} = 200 pF.

FIGURE 6. 1.5Mb/sec 10' Cable Driving Information



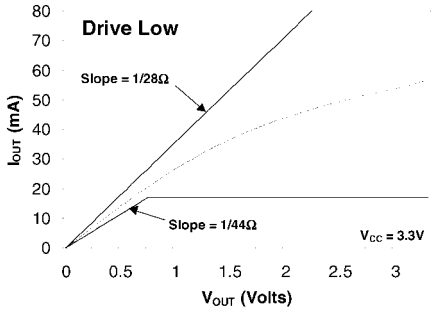
Note: Due to transmission line or cable effects, the Rise and Fall time in High Speed mode is measured between 0.8 and 2.5V.

FIGURE 7. 12Mb/sec 10' Cable Driving Information



Note: Includes 24Ω series output resistor.

FIGURE 8. Source Impedance High State



Note: 24Ω series output resistor

FIGURE 9. Source Impedance Low State

Transceiver Comparison

Actual performance and nearly identical product specifications should ease second source design considerations. However, the Fairchild USB1T11A has several advantages over similar USB transceivers.

1. Faster typical propagation delays
2. Slower edge rates
3. Lower conducted EMI
4. Enhanced ESD protection

The faster propagation delays allow additional time for the digital controller to process incoming and outgoing data before it is delivered to the USB transceiver.

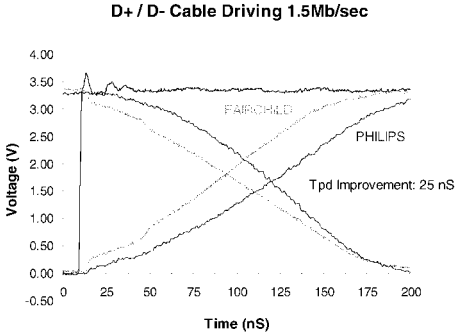


FIGURE 10. Transceiver t_{PD} Comparison

Controlled output edge rates reduce the overall transmission line effects and minimize signal degradation on the cable. This results in improved signal characteristics at the differential receiver.

Transceiver Comparison (Continued)

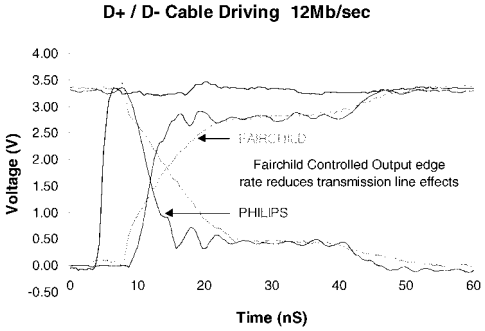
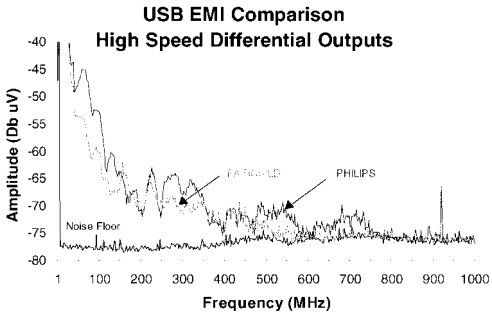


FIGURE 11. Controlled Output Edge Rate

EMI reduction at the system level is a major design challenge. USB components should work in harmony with the system to achieve the lowest possible level of EMI radiation ensuring that the entire system meets all FCC regulations. Although low device generated EMI can never guarantee low system EMI, using devices generating less EMI provides a solid foundation on which to build a system capable of passing FCC regulations.



Note: EMI measurements are taken at transceiver output driving 3m USB cable for a load. The fundamental frequency of the output is 1.0 MHz.

FIGURE 12. Conducted EMI

ELECTROSTATIC DISCHARGE

Electrostatic Discharge or ESD tolerance is especially important for USB transceivers. This type of device is connected directly to system I/O ports. Residing at the user interface often results in the need to absorb a transient ESD event as a USB function is attached or removed from the host system or USB hub.

TABLE 2. Transceiver ESD Performance:

Fairchild USB1T11A	4KV Minimum
Philips PDIUSBP11A	2KV Minimum
Mircrel MIC2550	Not Specified

The Fairchild USB Transceiver has already integrated effective ESD protection into the product. Therefore no external ESD protection is required for a robust USB interface implementation.

Conclusion

The Fairchild USB1T11A transceiver provides a low cost, low risk, and backward compatible solution to the analog signaling requirements of an USB 1.1 design.