High Efficiency Bidirectional Multicell Battery Balancer

FEATURES

- **Bidirectional Synchronous Flyback Balancing of Up to 6 Li-Ion or $LiFePO_4$ Cells in Series**
- **Up to 10A Balancing Current (Set by External Components)**
- **Bidirectional Architecture Minimizes Balancing Time and Power Dissipation**
- **Up to 92% Charge Transfer Efficiency**
- **Stackable Architecture Enables >1000V Systems**
- Uses Simple 2-Winding Transformers
- 1MHz Daisy-Chainable Serial Interface with 4-Bit CRC Packet Error Checking
- High Noise Margin Serial Communication
- Numerous Fault Protection Features
- 48-Lead Exposed Pad QFN and LQFP Packages

APPLICATIONS

- Electric Vehicles/Plug-in HEVs
- High Power UPS/Grid Energy Storage Systems
- General Purpose Multicell Battery Stacks

DESCRIPTION

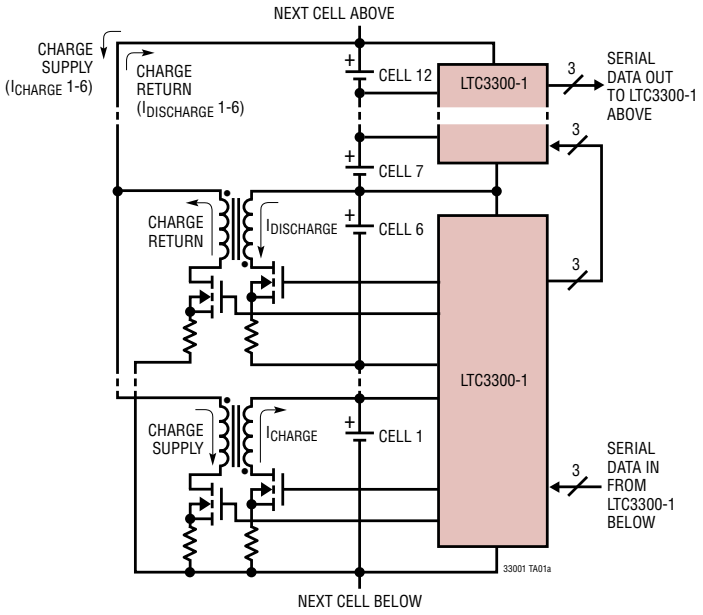
The LTC®3300-1 is a fault-protected controller IC for transformer-based bidirectional active balancing of multicell battery stacks. All associated gate drive circuitry, precision current sensing, fault detection circuitry and a robust serial interface with built-in watchdog timer are integrated.

Each LTC3300-1 can balance up to 6 series-connected battery cells with an input common mode voltage up to 36V. Charge from any selected cell can be transferred at high efficiency to or from 12 or more adjacent cells. A unique level-shifting SPI-compatible serial interface enables multiple LTC3300-1 devices to be connected in series, without opto-couplers or isolators, allowing for balancing of every cell in a long string of series-connected batteries.

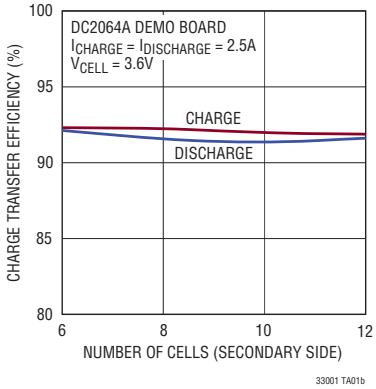
When multiple LTC3300-1 devices are connected in series they can operate simultaneously, permitting all cells in the stack to be balanced concurrently and independently. Fault protection features include readback capability, cyclic redundancy check (CRC) error detection, maximum on-time volt-second clamps, and overvoltage shutoffs.

TYPICAL APPLICATION

High Efficiency Bidirectional Balancing



Balancer Efficiency

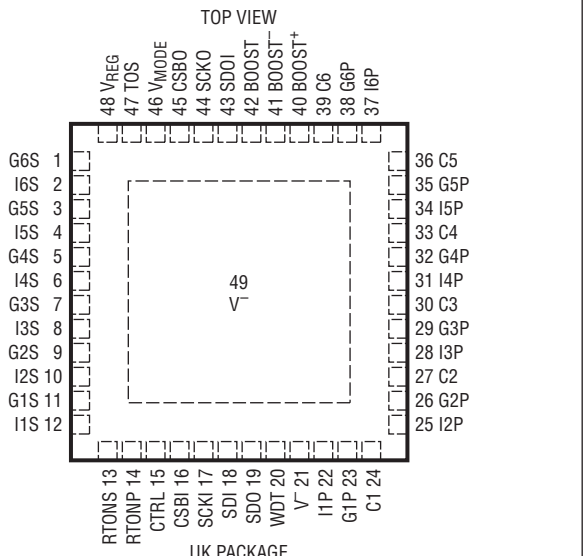


ABSOLUTE MAXIMUM RATINGS (Note 1)

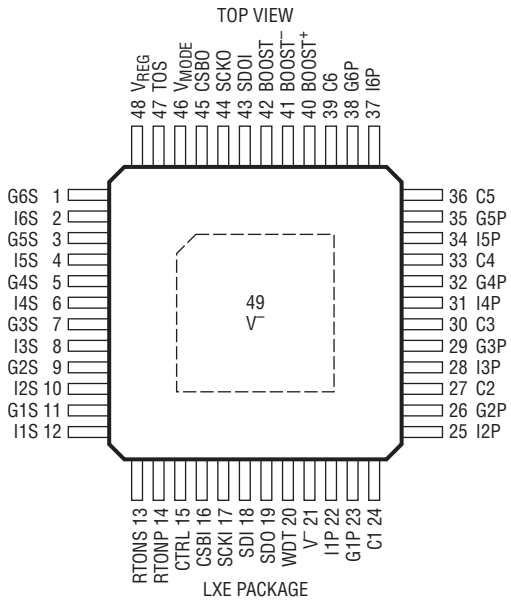
Total Supply Voltage (C6 to V^-).....36V
Input Voltage (Relative to V^-)
C1 .....–0.3V to 6V
I1P .....–0.3V to 0.3V
I1S, I2S, I3S, I4S, I5S, I6S.....–0.3V to 0.3V
CSBI, SCKI, SDI .....–0.3V to 6V
CSBO, SCKO, SDOI .....–0.3V to 36V
V_{REG}, SDO .....–0.3V to 6V
RTONP, RTONS.....–0.3V to Min[V_{REG} + 0.3V, 6V]
TOS, V_{MODE}, CTRL,
BOOST, WDT .....–0.3V to Min[V_{REG} + 0.3V, 6V]

Voltage Between Pins
C*n* to C*n-1**.....–0.3V to 6V
I*n*P to C*n-1**.....–0.3V to 0.3V
BOOST$^+$ to C6 .....–0.3V to 6V
CSBO to SCKO, CSBO to SDOI,
SCKO to SDOI .....–0.3V to 0.3V
SDO Current.....10mA
G1P, G*n*P, G1S, G*n*S, BOOST$^-$ Current..... ±200mA
Operating Junction Temperature Range (Notes 2, 7)
LTC3300I-1 .....–40°C to 125°C
LTC3300H-1.....–40°C to 150°C
Storage Temperature Range .....–65°C to 150°C
**n* = 2 to 6

PIN CONFIGURATION



UK PACKAGE
48-LEAD (7mm × 7mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 34°C/W, θ_{JC} = 3°C/W
EXPOSED PAD (PIN 49) IS V^-, MUST BE SOLDERED TO PCB



LXE PACKAGE
48-LEAD (7mm × 7mm) PLASTIC LQFP
T_{JMAX} = 150°C, θ_{JA} = 20.46°C/W, θ_{JC} = 3.68°C/W
EXPOSED PAD (PIN 49) IS V^-, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3300IUK-1#PBF	LTC3300IUK-1#TRPBF	LTC3300UK-1	48-Lead (7mm × 7mm) Plastic QFN	–40°C to 125°C
LTC3300HUK-1#PBF	LTC3300HUK-1#TRPBF	LTC3300UK-1	48-Lead (7mm × 7mm) Plastic QFN	–40°C to 150°C
LTC3300ILXE-1#PBF	LTC3300ILXE-1#TRPBF	LTC3300LXE-1	48-Lead (7mm × 7mm) Plastic eLQFP	–40°C to 125°C
LTC3300HLXE-1#PBF	LTC3300HLXE-1#TRPBF	LTC3300LXE-1	48-Lead (7mm × 7mm) Plastic eLQFP	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2) BOOST⁺ = 25.2V, C6 = 21.6V, C5 = 18V, C4 = 14.4V, C3 = 10.8V, C2 = 7.2V, C1 = 3.6V, V⁻ = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC Specifications							
I_{Q_SD}	Supply Current When Not Balancing (Post Suspend or Pre First Execute)	Measured at C1, C2, C3, C4, C5			0	1	µA
		Measured at C6		7	16	25	µA
		Measured at BOOST⁺			0	10	µA
I_{Q_ACTIVE}	Supply Current When Balancing (Note 3)	Balancing C1 Only (Note 4 for V⁻, C2, C6)					
		Measured at C1			250	375	µA
		Measured at C2, C3, C4, C5			70	105	µA
		Measured at C6			560	840	µA
		Measured at BOOST⁺			0	10	µA
		Balancing C2 Only (Note 4 for C1, C3, C6)					
		Measured at C1		–105	–70		µA
		Measured at C2			250	375	µA
		Measured at C3, C4, C5			70	105	µA
		Measured at C6			560	840	µA
		Measured at BOOST⁺			0	10	µA
		Balancing C3 Only (Note 4 for C2, C4, C6)					
		Measured at C1, C4, C5			70	105	µA
		Measured at C2		–105	–70		µA
		Measured at C3			250	375	µA
		Measured at C6			560	840	µA
		Measured at BOOST⁺			0	10	µA
		Balancing C4 Only (Note 4 for C3, C5, C6)					
		Measured at C1, C2, C5			70	105	µA
		Measured at C3		–105	–70		µA
		Measured at C4			250	375	µA
		Measured at C6			560	840	µA
		Measured at BOOST⁺			0	10	µA
		Balancing C5 Only (Note 4 for C4, C6)					
		Measured at C1, C2, C3			70	105	µA
		Measured at C4		–105	–70		µA
		Measured at C5			250	375	µA
		Measured at C6			560	840	µA
		Measured at BOOST⁺			0	10	µA
		Balancing C6 Only (Note 4 for C5, C6, BOOST⁺)					
		Measured at C1, C2, C3, C4			70	105	µA
		Measured at C5		–105	–70		µA
		Measured at C6			740	1110	µA
		Measured at BOOST⁺ (BOOST = V⁻)			60	90	µA
		Measured at BOOST⁺ (BOOST = V_{REG})			0	10	µA

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{Q_EXTRA}	Supply Current Extra (Serial I/O in Current Mode)	Additional Current Measured at C6, V_{MODE} = V⁻ (CSBI Logic Low, SCKI and SDI Both Logic High; Refer to I_{IL1}, I_{IH1}, I_{OH1}, I_{OL1} Specs)			3.75		mA
$V_{CELL\|MIN}$	Minimum Cell Voltage (Rising) Required for Primary Gate Drive	C*n* to C*n* – *1* Voltage to Balance C*n*, *n* = 2 to 6 C1 Voltage to Balance C1 C*n* + 1 to C*n* Voltage to Balance C*n*, *n* = 1 to 5 BOOST⁺ to C6 Voltage to Balance C6, BOOST = V⁻	● ● ● ●	1.8 1.8 1.8 1.8	2 2 2 2	2.2 2.2 2.2 2.2	V V V V
$V_{CELL\|MIN(HYST)}$	$V_{CELL\|MIN}$ Comparator Hysteresis				70		mV
$V_{CELL\|MAX}$	Maximum Cell Voltage (Rising) Before Disabling Balancing	C1, C*n* to C*n* – *1* Voltage to Balance Any Cell, *n* = 2 to 6	●	4.7	5	5.3	V
$V_{CELL\|MAX(HYST)}$	$V_{CELL\|MAX}$ Comparator Hysteresis				0.5		V
$V_{CELL\|RECONNECT}$	Maximum Cell Voltage (Falling) to Re-Enable Balancing		●	4.25			V
V_{REG}	Regulator Pin Voltage	9V ≤ C6 ≤ 36V, 0mA ≤ I_{LOAD} ≤ 20mA	●	4.4	4.8	5.2	V
$V_{REG\|POR}$	V_{REG} Voltage (Rising) for Power-On Reset				4.0		V
$V_{REG\|MIN}$	Minimum V_{REG} Voltage (Falling) for Secondary Gate Drive	V_{REG} Voltage to Balance C*n*, *n* = 1 to 6	●	3.8			V
I_{REG_SC}	Regulator Pin Short Circuit Current Limit	V_{REG} = 0V			55		mA
V_{RTONP}	RTONP Servo Voltage	R_{RTONP} = 20kΩ	●	1.158	1.2	1.242	V
V_{RTONS}	RTONS Servo Voltage	R_{RTONS} = 15kΩ	●	1.158	1.2	1.242	V
I_{WDT_RISING}	WDT Pin Current, Balancing	R_{TONS} = 15kΩ, WDT = 0.5V	●	72	80	88	µA
$I_{WDT\_FALLING}$	WDT Pin Current as a Percentage of I_{WDT_RISING}, Secondary OV	R_{TONS} = 15kΩ, WDT = 2V	●	85	87.5	90	%
V_{PEAK_P}	Primary Winding Peak Current Sense Voltage	I1P I*n*P to C*n* – *1*, *n* = 2 to 6	● ●	45 45	50 50	55 55	mV mV
	V_{PEAK_P} Matching (All 6)	±[(Max – Min)/(Max + Min)] • 100%	●		±1.7	±5	%
V_{PEAK_S}	Secondary Winding Peak Current Sense Voltage	I1S I*n*S to C*n* – *1*, *n* = 2 to 6, CTRL = 0 Only	● ●	45 45	50 50	55 55	mV mV
	V_{PEAK_S} Matching (All 6)	±[(Max – Min)/(Max + Min)] • 100%	●		±0.5	±3	%
V_{ZERO_P}	Primary Winding Zero Current Sense Voltage (Note 5)	I1P I*n*P to C*n* – *1*, *n* = 2 to 6	● ●	–7 –7	–2 –2	3 3	mV mV
	V_{ZERO_P} Matching (All 6) Normalized to Mid-Range V_{PEAK_P}	±{[(Max – Min)/2]/($V_{PEAK\_P\|MIDRANGE}$)} • 100% (Note 6)	●		±1.7	±5	%
V_{ZERO_S}	Secondary Winding Zero Current Sense Voltage (Note 5)	I1S I*n*S to C*n* – 1, *n* = 2 to 6, CTRL = 0 Only	● ●	–12 –12	–7 –7	–2 –2	mV mV
	V_{ZERO_S} Matching (All 6) Normalized to Mid-Range V_{PEAK_S}	±{[(Max – Min)/2]/($V_{PEAK\_S\|MIDRANGE}$)} • 100% (Note 6)	●		±0.5	±3	%
R_{BOOST_L}	BOOST⁻ Pin Pull-Down R_{ON}	Measured at 100mA Into Pin, BOOST = V_{REG}			2.5		Ω
R_{BOOST_H}	BOOST⁻ Pin Pull-Up R_{ON}	Measured at 100mA Out of Pin, BOOST = V_{REG}			4		Ω
T_{SD}	Thermal Shutdown Threshold (Note 7)	Rising Temperature			155		°C
T_{HYS}	Thermal Shutdown Hysteresis				10		°C
Timing Specifications							
t_{r_P}	Primary Winding Gate Drive Rise Time (10% to 90%)	G1P Through G6P, C_{GATE} = 2500pF			35	70	ns
t_{f_P}	Primary Winding Gate Drive Fall Time (90% to 10%)	G1P Through G6P, C_{GATE} = 2500pF			20	40	ns

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{r_S}	Secondary Winding Gate Drive Rise Time (10% to 90%)	G1S, C_{GATE} = 2500pF G2S Through G6S, CTRL = 0 Only, C_{GATE} = 2500pF			30 30	60 60	ns ns
t_{f_S}	Secondary Winding Gate Drive Fall Time (90% to 10%)	G1S, C_{GATE} = 2500pF G2S Through G6S, CTRL = 0 Only, C_{GATE} = 2500pF			20 20	40 40	ns ns
$t_{ONP\|MAX}$	Primary Winding Switch Maximum On-Time	R_{RTONP} = 20kΩ (Measured at G1P-G6P)	●	6	7.2	8.4	µs
	$t_{ONP\|MAX}$ Matching (All 6)	±[(Max – Min)/(Max + Min)] • 100%	●		±1	±4	%
$t_{ONS\|MAX}$	Secondary Winding Switch Maximum On-Time	R_{RTONS} = 15kΩ (Measured at G1S-G6S)	●	1	1.2	1.4	µs
	$t_{ONS\|MAX}$ Matching (All 6)	±[(Max – Min)/(Max + Min)] • 100%	●		±1	±4	%
t_{DLY_START}	Delayed Start Time After New/ Different Balance Command or Recovery from Voltage/Temp Fault				2		ms
Voltage Mode Timing Specifications							
t_1	SDI Valid to SCKI Rising Setup	Write Operation	●	10			ns
t_2	SDI Valid from SCKI Rising Hold	Write Operation	●	250			ns
t_3	SCKI Low		●	400			ns
t_4	SCKI High		●	400			ns
t_5	CSBI Pulse Width		●	400			ns
t_6	SCKI Rising to CSBI Rising		●	100			ns
t_7	CSBI Falling to SCKI Rising		●	100			ns
t_8	SCKI Falling to SDO Valid	Read Operation	●			250	ns
f_{CLK}	Clock Frequency		●			1	MHz
t_{WD1}	Watchdog Timer Timeout Period	WDT Assertion Measured from Last Valid Command Byte	●	0.75	1.5	2.25	second
t_{WD2}	Watchdog Timer Reset Time	WDT Negation Measured from Last Valid Command Byte	●		1.5	5	µs
Current Mode Timing Specifications							
t_{PD1}	CSBI to CSBO Delay	C_{CSBO} = 150pF	●			600	ns
t_{PD2}	SCKI Rising to SCKO Delay	C_{SCKO} = 150pF	●			300	ns
t_{PD3}	SDI to SDOI Delay	C_{SDOI} = 150pF, Command Byte	●			300	ns
t_{PD4}	SCKI Falling to SDOI Valid	C_{SDOI} = 150pF, Write Balance Command	●			300	ns
t_{PD5}	SCKI Falling to SDI Valid	C_{SDI} = 150pF, Read Operation	●			300	ns
t_{SCKO}	SCKO Pulse Width	C_{SCKO} = 150pF			100		ns
Voltage Mode Digital I/O Specifications							
V_{IH}	Digital Input Voltage High	Pins CSBI, SCKI, SDI; V_{MODE} = V_{REG} Pins CTRL, BOOST, V_{MODE}, TOS Pin WDT	● ● ●	V_{REG} – 0.5 V_{REG} – 0.5 2			V V V
V_{IL}	Digital Input Voltage Low	Pins CSBI, SCKI, SDI; V_{MODE} = V_{REG} Pins CTRL, BOOST, V_{MODE}, TOS Pin WDT	● ● ●			0.5 0.5 0.8	V V V
I_{IH}	Digital Input Current High	Pins CSBI, SCKI, SDI; V_{MODE} = V_{REG} Pins CTRL, BOOST, V_{MODE}, TOS Pin WDT, Timed Out		–1 –1 –1	0 0 0	1 1 1	µA µA µA
I_{IL}	Digital Input Current Low	Pins CSBI, SCKI, SDI; V_{MODE} = V_{REG} Pins CTRL, BOOST, V_{MODE}, TOS Pin WDT, Not Balancing		–1 –1 –1	0 0 0	1 1 1	µA µA µA

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OL}	Digital Output Voltage Low	Pin SDO, Sinking 500µA; $V_{MODE} = V_{REG}$; Read	●			0.3	V
I_{OH}	Digital Output Current High	Pin SDO at 6V	●			100	nA
Current Mode Digital I/O Specifications							
I_{IL1}	Digital Input Current Low	Pin CSBI; $V_{MODE} = V^-$	●	–1500	–1250	–1000	µA
		Pin SCKI; $V_{MODE} = V^-$	●	–5	–2.5	0	µA
		Pin SDI, $V_{MODE} = V^-$, Write	●	–5	–2.5	0	µA
		Pin SDOI, TOS = V^-, Read	●	0	2.5	5	µA
I_{IH1}	Digital Input Current High	Pin CSBI; $V_{MODE} = V^-$	●	–5	–2.5	0	µA
		Pin SCKI; $V_{MODE} = V^-$	●	–1500	–1250	–1000	µA
		Pin SDI, $V_{MODE} = V^-$, Write	●	–1500	–1250	–1000	µA
		Pin SDOI, TOS = V^-, Read	●	1000	1250	1500	µA
I_{OH1}	Digital Output Current High	Pin CSBO; TOS = V^-	●	0	2.5	5	µA
		Pin SCKO; TOS = V^-	●	1000	1250		µA
		Pin SDOI, TOS = V^-, Write	●	1000	1250		µA
		Pin SDI, $V_{MODE} = V^-$, Read	●			–1000	µA
I_{OL1}	Digital Output Current Low	Pin CSBO; TOS = V^-	●	1000	1250		µA
		Pin SCKO; TOS = V^-	●	0	2.5	5	µA
		Pin SDOI, TOS = V^-, Write	●	0	2.5	5	µA
		Pin SDI, $V_{MODE} = V^-$, Read	●	–5			µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3300-1 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3300I-1 is guaranteed over the –40°C to 125°C operating junction temperature range and the LTC3300H-1 is guaranteed over the –40°C to 150°C operating junction temperature. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where θ_{JA} (in °C/W) is the package thermal impedance.

Note 3: When balancing more than one cell at a time, the individual cell supply currents can be calculated from the values given in the table as follows: First add the appropriate table entries cell by cell for the balancers that are on. Second, *for each additional balancer that is on*, subtract 70µA from the resultant sums for C1, C2, C3, C4, and C5, and 450µA from the resultant sum for C6. For example, if all six balancers are on, the resultant current for C1 is [250 – 70 + 70 + 70 + 70 + 70 – 5(70)]µA = 110µA and for C6 is [560 + 560 + 560 + 560 + 560 + 740 – 5(450)]µA = 1290µA.

Note 4: Dynamic supply current is higher due to gate charge being delivered at the switching frequency during active balancing. See Gate Drivers/Gate Drive Comparators and Voltage Regulator in the Operation section for more information on estimating these currents.

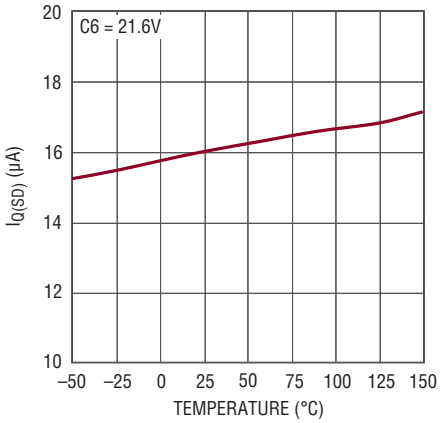
Note 5: The zero current sense voltages given in the table are DC thresholds. The actual zero current sense voltage seen in application will be closer to zero due to the slew rate of the winding current and the finite delay of the current sense comparator.

Note 6: The mid-range value is the average of the minimum and maximum readings within the group of six.

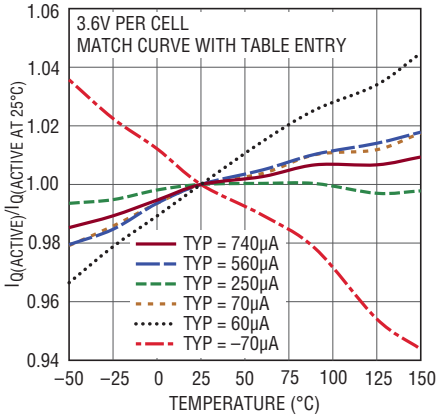
Note 7: This IC includes overtemperature protection intended to protect the device during momentary overload conditions. The maximum junction temperature may be exceeded when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise specified.

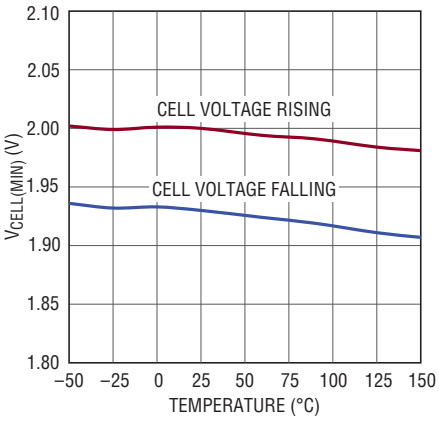
C6 Supply Current When Not Balancing vs Temperature



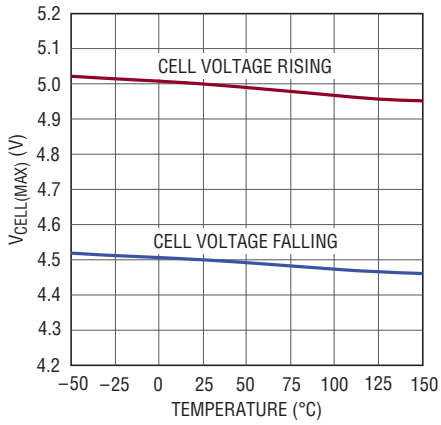
Supply Current When Balancing vs Temperature Normalized to 25°C



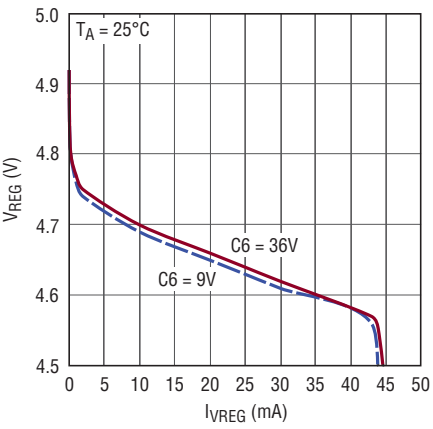
Minimum Cell Voltage Required for Primary Gate Drive vs Temperature



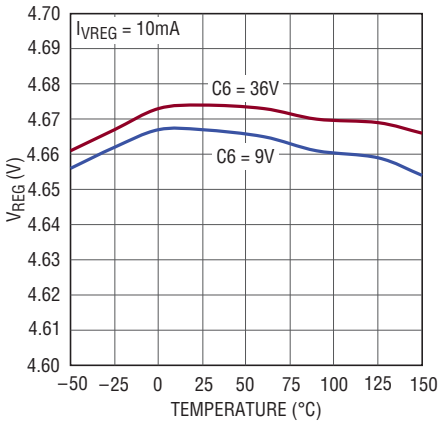
Maximum Cell Voltage to Allow Balancing vs Temperature



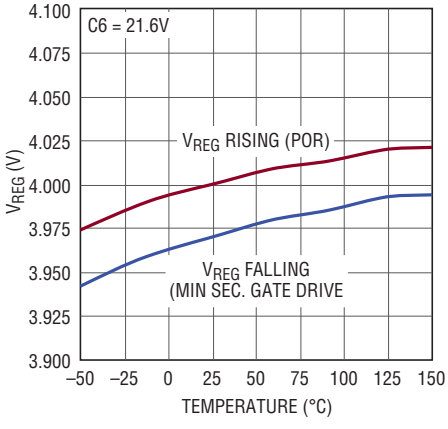
V_{REG} Load Regulation



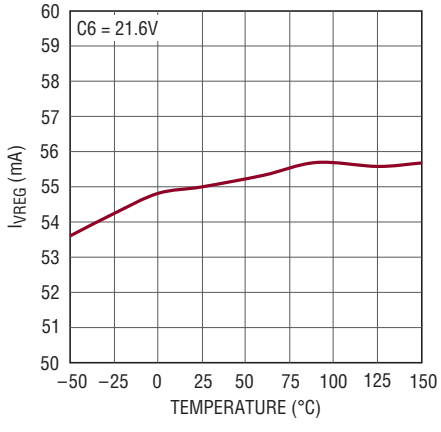
V_{REG} Voltage vs Temperature



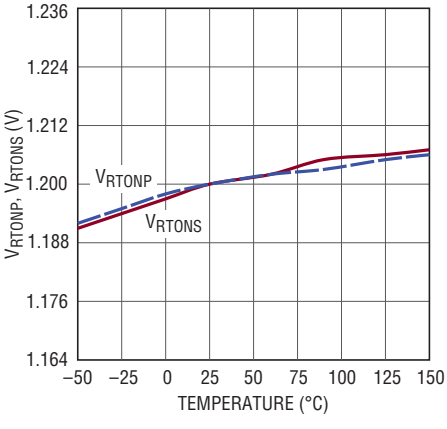
V_{REG} POR Voltage and Minimum Secondary Gate Drive vs Temperature



V_{REG} Short-Circuit Current Limit vs Temperature

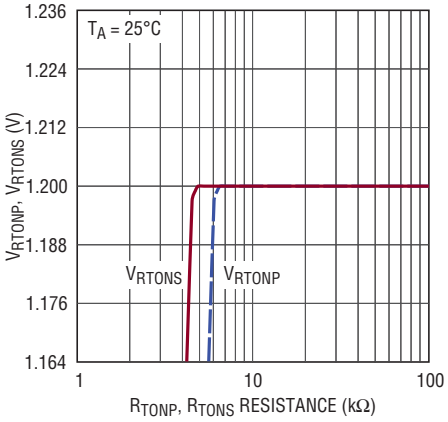


V_{RTONP}, V_{RTONS} vs Temperature

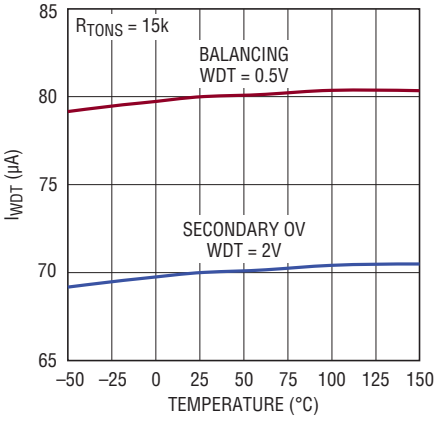


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise specified.

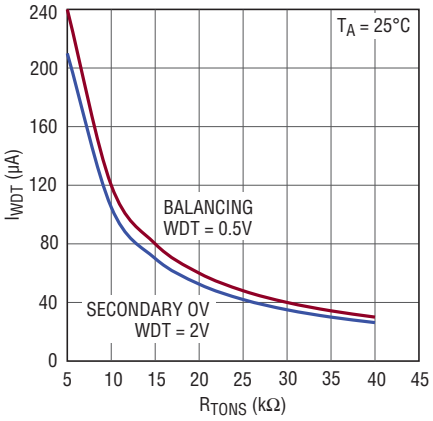
V_{RTONP}, V_{RTONS} vs External Resistance



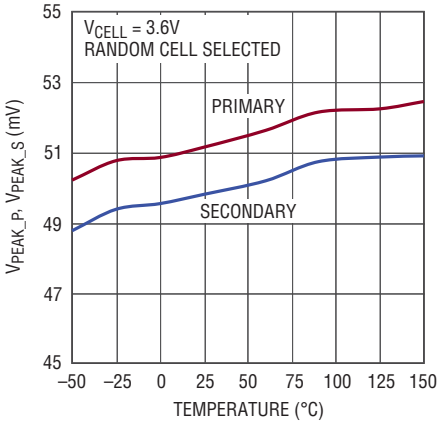
WDT Pin Current vs Temperature



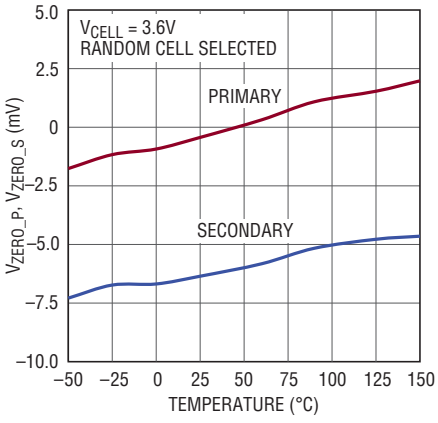
WDT Pin Current vs R_{TONS}



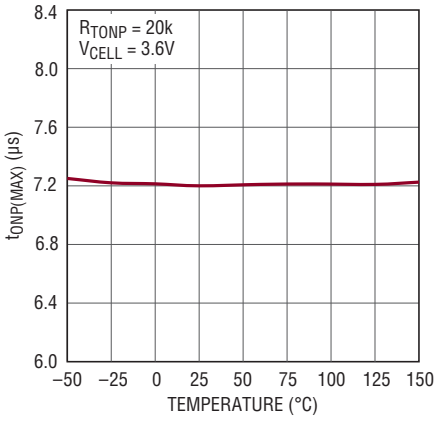
Peak Current Sense Threshold vs Temperature



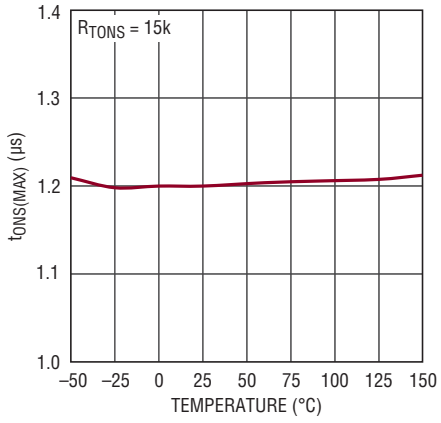
Zero Current Sense Threshold vs Temperature



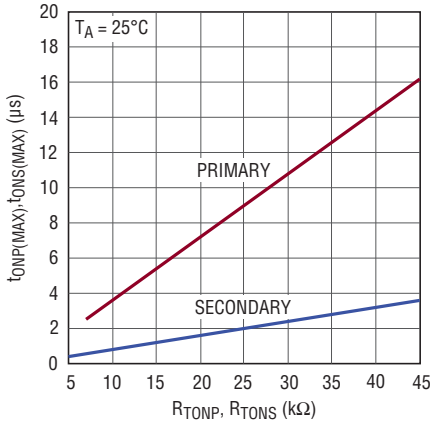
Primary Winding Switch Maximum On-Time vs Temperature



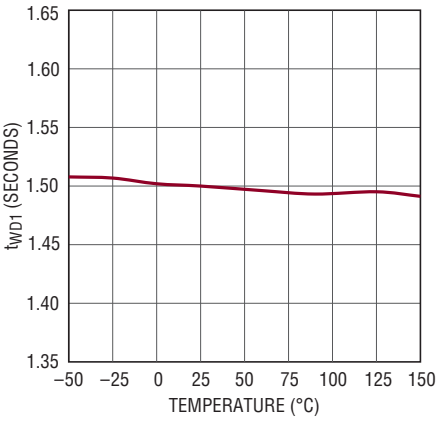
Secondary Winding Switch Maximum On-Time vs Temperature



Maximum On-Time vs R_{TONP}, R_{TONS}

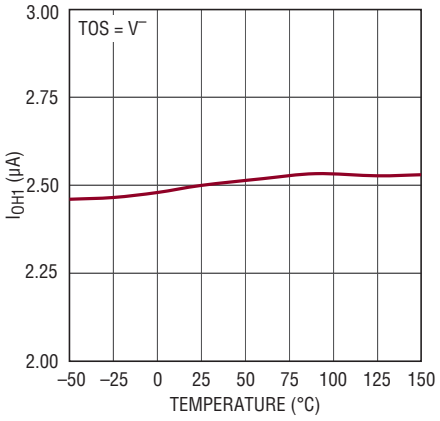


Watchdog Timer Timeout Period vs Temperature

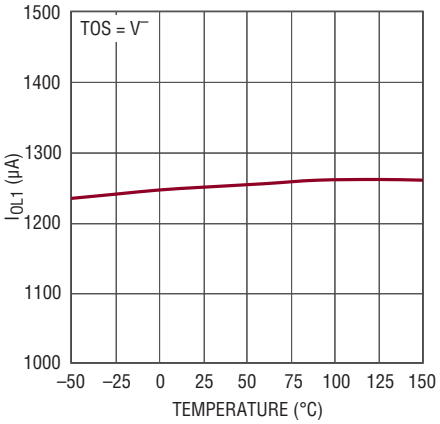


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise specified.

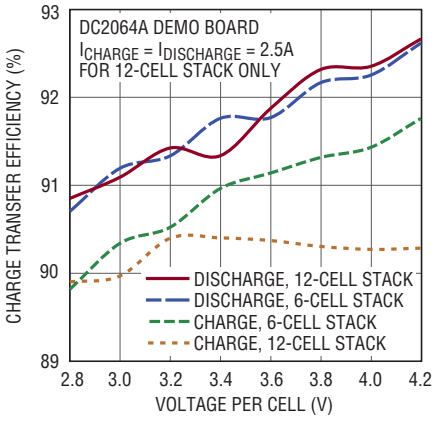
CSBO Digital Output Current High vs Temperature



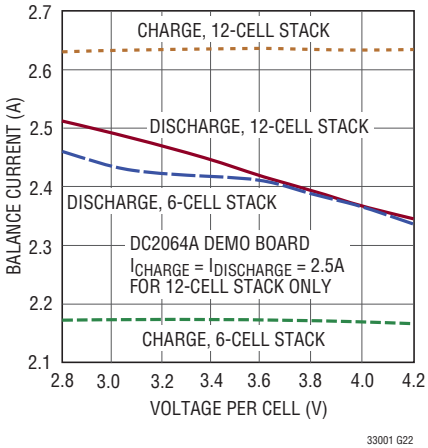
CSBO Digital Output Current Low vs Temperature



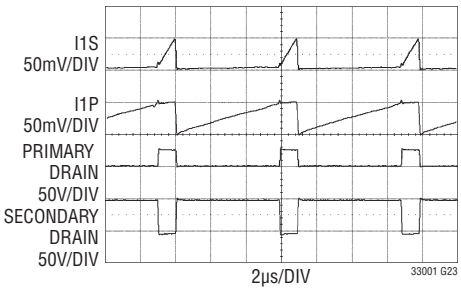
Balancer Efficiency vs Cell Voltage



Balance Current vs Cell Voltage

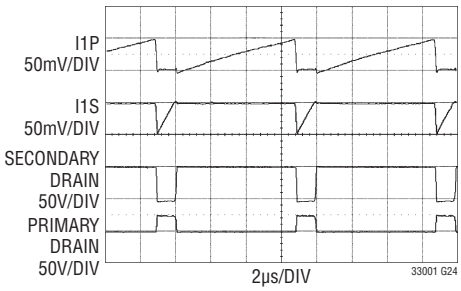


Typical Charge Waveforms



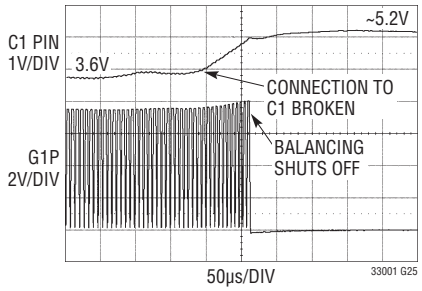
DC2064A DEMO BOARD
I_{CHARGE} = 2.5A
T = 2
S = 12

Typical Discharge Waveforms

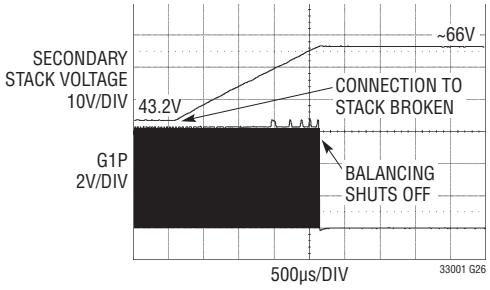


DC2064A DEMO BOARD
$I_{DISCHARGE}$ = 2.5A
T = 2
S = 12

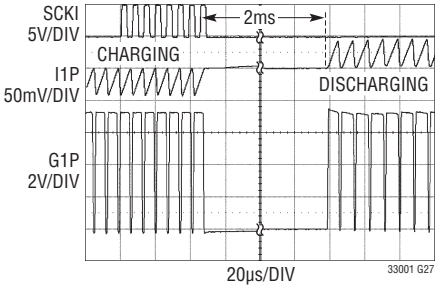
Protection for Broken Connection to Cell While Charging



Protection for Broken Connection to Secondary Stack While Discharging



Changing Balancer Direction "On the Fly"



PIN FUNCTIONS

Note: The convention adopted in this data sheet is to refer to the transformer winding paralleling an individual battery cell as the primary and the transformer winding paralleling multiple series-stacked cells as the secondary, *regardless of the direction of energy transfer.*

G6S, G5S, G4S, G3S, G2S, G1S (Pins 1, 3, 5, 7, 9, 11): G1S through G6S are gate driver outputs for driving external NMOS transistors connected in series with the secondary windings of transformers whose primaries are connected in parallel with battery cells 1 through 6. For the minimum part count balancing application employing a single transformer (CTRL = V_{REG}), G2S through G6S are no connects.

I6S, I5S, I4S, I3S, I2S, I1S (Pins 2, 4, 6, 8, 10, 12): I1S through I6S are current sense inputs for measuring secondary winding current in transformers whose primaries are connected in parallel with battery cells 1 through 6. For the minimum part count balancing application employing a single transformer (CTRL = V_{REG}), I2S through I6S should be tied to V^-.

RTONS (Pin 13): Secondary Winding Max t_{ON} Setting Resistor. The RTONS pin servos to 1.2V. A resistor to V^- programs the maximum on-time for all external NMOS transistors connected in series with secondary windings. This protects against a short-circuited current sense resistor in any secondary winding. To defeat this function, connect RTONS to V_{REG}. The secondary winding OVP threshold (see WDT pin) is also slaved to the value of the R_{TONS} resistor.

RTONP (Pin 14): Primary Winding Max t_{ON} Setting Resistor. The RTONP pin servos to 1.2V. A resistor to V^- programs the maximum on-time for all external NMOS transistors connected in series with primary windings. This protects against a short-circuited current sense resistor in any primary winding. To defeat this function, connect RTONP to V_{REG}.

CTRL: (Pin 15): Control Input. The CTRL pin configures the LTC3300-1 for the minimum part count application employing a single transformer if CTRL is tied to V_{REG} or for the multiple transformer application if CTRL is tied to V^-. This pin must be tied to either V_{REG} or V^-.

CSBI (Pin 16): Chip Select (Active Low) Input. The CSBI pin interfaces to a rail-to-rail output logic gate if V_{MODE} is tied to V_{REG}. CSBI must be driven by the CSBO pin of another LTC3300-1 if V_{MODE} is tied to V^-. See Serial Port in the Applications Information section.

SCKI (Pin 17): Serial Clock Input. The SCKI pin interfaces to a rail-to-rail output logic gate if V_{MODE} is tied to V_{REG}. SCKI must be driven by the SCKO pin of another LTC3300-1 if V_{MODE} is tied to V^-. See Serial Port in the Applications Information section.

SDI (Pin 18): Serial Data Input. When writing data to the LTC3300-1, the SDI pin interfaces to a rail-to-rail output logic gate if V_{MODE} is tied to V_{REG} or must be driven by the SDOI pin of another LTC3300-1 if V_{MODE} is tied to V^-. See Serial Port in the Applications Information section.

SDO (Pin 19): Serial Data Output. When reading data from the LTC3300-1, the SDO pin is an NMOS open-drain output if V_{MODE} is tied to V_{REG}. The SDO pin is not used if V_{MODE} is tied to V^-. See Serial Port in the Applications Information section.

WDT (Pin 20): Watchdog Timer Output (Active High). At initial power-up and when not attempting to execute a valid balance command, the WDT pin is high impedance and will be pulled high (internally clamped to ~5.6V) if an external pull-up resistor is present. While balancing (or attempting to balance but not able to due to voltage/temperature faults) and during normal communication activity, the WDT pin is pulled low by a precision current source slaved to the R_{TONS} resistor. However, if no valid command byte is written for 1.5 seconds (typical), the WDT output will go back high. When WDT is high, all balancers are off. The watchdog timer function can be disabled by connecting WDT to V^-. The secondary winding OVP function can also be implemented using this pin (See Operation section).

V^- (Pin 21): Connect V^- to the most negative potential in the series of cells.

I1P, I2P, I3P, I4P, I5P, I6P (Pins 22, 25, 28, 31, 34, 37): I1P through I6P are current sense inputs for measuring primary winding current in transformers connected in parallel with battery cells 1 through 6.

PIN FUNCTIONS

G1P, G2P, G3P, G4P, G5P, G6P (Pins 23, 26, 29, 32, 35, 38): G1P through G6P are gate driver outputs for driving external NMOS transistors connected in series with the primary windings of transformers connected in parallel with battery cells 1 through 6.

C1, C2, C3, C4, C5, C6 (Pins 24, 27, 30, 33, 36, 39): C1 through C6 connect to the positive terminals of battery cells 1 through 6. Connect the negative terminal of battery cell 1 to V^-.

BOOST$^+$ (Pin 40): Boost$^+$ Pin. Connects to the anode of the external flying capacitor used for generating sufficient gate drive necessary for balancing the topmost battery cell in a given LTC3300-1 sub-stack. A Schottky diode from C6 to BOOST$^+$ is needed as well. Alternately, the BOOST$^+$ pin can connect to one cell up in the above sub-stack (if present). This pin is effectively C7. (Note: "Sub-stack" refers to the 3-6 battery cells connected locally to an individual LTC3300-1 as part of a larger stack.)

BOOST$^-$ (Pin 41): Boost$^-$ Pin. Connects to the cathode of the external flying capacitor used for generating sufficient gate drive necessary for balancing the topmost battery cell in a given LTC3300-1 sub-stack. Alternately, if the BOOST$^+$ pin connects to the next higher cell in the above sub-stack (if present), this pin is a no connect.

BOOST (Pin 42): Enable Boost Pin. Connect BOOST to V_{REG} to enable the boosted gate drive needed for balancing the top cell in a given LTC3300-1 sub-stack. If the BOOST$^+$ pin can be connected to the next cell up in the stack (i.e., C1 of the next LTC3300-1 in the stack), then BOOST should be tied to V^- and BOOST$^-$ no connected. This pin must be tied to either V_{REG} or V^-.

SDOI (Pin 43): Serial Data Output/Input. SDOI transfers data to and from the next IC higher in the daisy chain when writing and reading. See Serial Port in the Applications Information section.

SCKO (Pin 44): Serial Clock Output. SCKO is a buffered and one-shotted version of the serial clock input, SCKI, when CSBI is low. SCKO drives the next IC higher in the daisy chain. See Serial Port in the Applications Information section.

CSBO (Pin 45): Chip Select (Active Low) Output. CSBO is a buffered version of the chip select input, CSBI. CSBO drives the next IC higher in the daisy chain. See Serial Port in the Applications Information section.

V_{MODE} (Pin 46): Voltage Mode Input. When V_{MODE} is tied to V_{REG}, the CSBI, SCKI, SDI and SDO pins are configured as voltage inputs and outputs. This means these pins accept V_{REG}-referred rail-to-rail logic levels. Connect V_{MODE} to V_{REG} when the LTC3300-1 is the bottom device in a daisy chain.

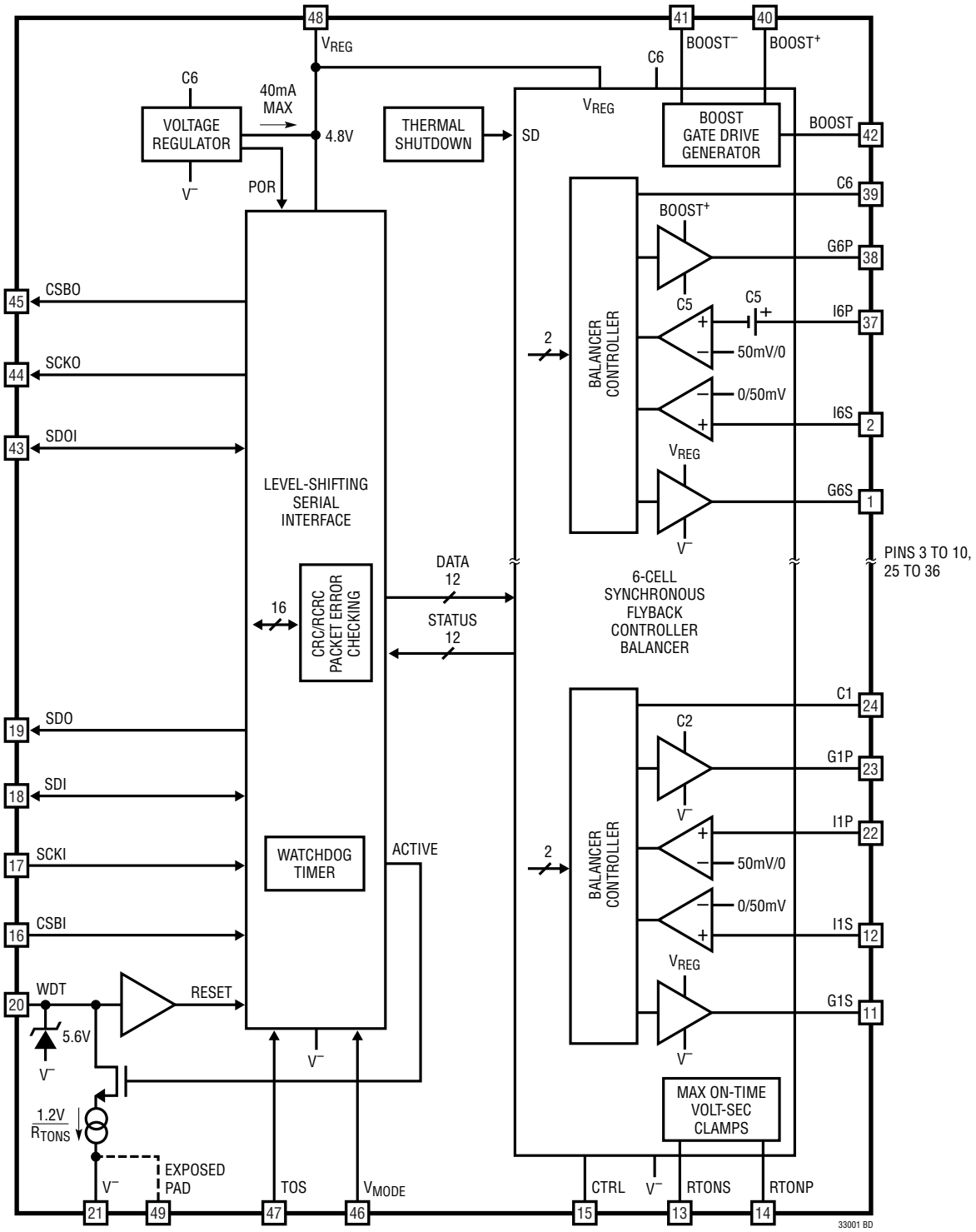
When V_{MODE} is tied to V^-, the CSBI, SCKI and SDI pins are configured as current inputs and outputs, and SDO is unused. Connect V_{MODE} to V^- when the LTC3300-1 is being driven by another LTC3300-1 lower in the daisy chain. This pin must be tied to either V_{REG} or V^-.

TOS (Pin 47): Top Of Stack Input. Tie TOS to V_{REG} when the LTC3300-1 is the top device in a daisy chain. Tie TOS to V^- when the LTC3300-1 is any other device in the daisy chain. When TOS is tied to V_{REG}, the LTC3300-1 ignores the SDOI input. When TOS is tied to V^-, the LTC3300-1 expects data to be passed to and from the SDOI pin. This pin must be tied to either V_{REG} or V^-.

V_{REG} (Pin 48): Linear Voltage Regulator Output. This 4.8V output should be bypassed with a 1µF or larger capacitor to V^-. The V_{REG} pin is capable of supplying up to 40mA to internal and external loads. The V_{REG} pin does not sink current.

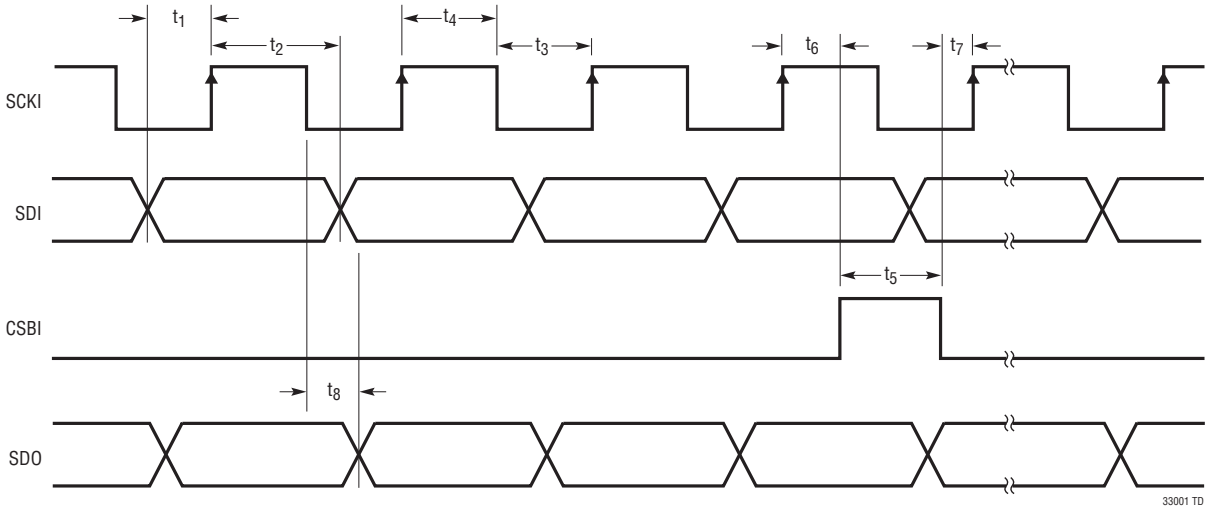
V^- (Exposed Pad Pin 49): The exposed pad should be connected to a continuous (ground) plane biased at V^- on the second layer of the printed circuit board by several vias directly under the LTC3300-1.

BLOCK DIAGRAM



TIMING DIAGRAM

Timing Diagram of the Serial Interface



OPERATION

Battery Management System (BMS)

The LTC3300-1 multicell battery cell balancer is a key component in a high performance battery management system (BMS) for series-connected Li-Ion cells. It is designed to operate in conjunction with a monitor, a charger, and a microprocessor or microcontroller (see Figure 1).

The function of the balancer is to efficiently transfer charge to/from a given out-of-balance cell in the stack from/to a larger group of neighboring cells (which includes that individual cell) in order to bring that cell into voltage or capacity balance with its neighboring cells. Ideally, this charge would always be transferred directly from/to the entire stack, but this is impractical for voltage reasons when the number of cells in the overall stack is large. The LTC3300-1 is designed to interface to a group of up to 6 series cells, so the number of LTC3300-1 ICs required to balance a series stack of N cells is N/6 rounded up to the nearest integer, with no limitation imposed on how large N can be. For connecting an individual LTC3300-1 in the stack to fewer than 6 cells, refer to the Applications Information section.

Because the balancing function entails switching large (multiampere) currents between cells, precision voltage monitoring in the BMS is better served by a dedicated monitor component such as the LTC6803-1 or one of its family of parts. The LTC6803-1 provides for high precision A/D monitoring of up to 12 series cells. The only voltage monitoring provided by the LTC3300-1 is a coarse "out-of-range" overvoltage and undervoltage cell balancing disqualification, which provides a safety shutoff in the event Kelvin sensing to the monitor component is lost.

In the process of bringing the cells into balance, the overall stack is slightly discharged. The charger component provides a means for net charging of the entire stack from an alternate power source.

The last component in the BMS is a microprocessor/microcontroller which communicates directly with the balancer, monitor, and charger to receive voltage, current, and temperature information and to implement a balancing algorithm.

OPERATION

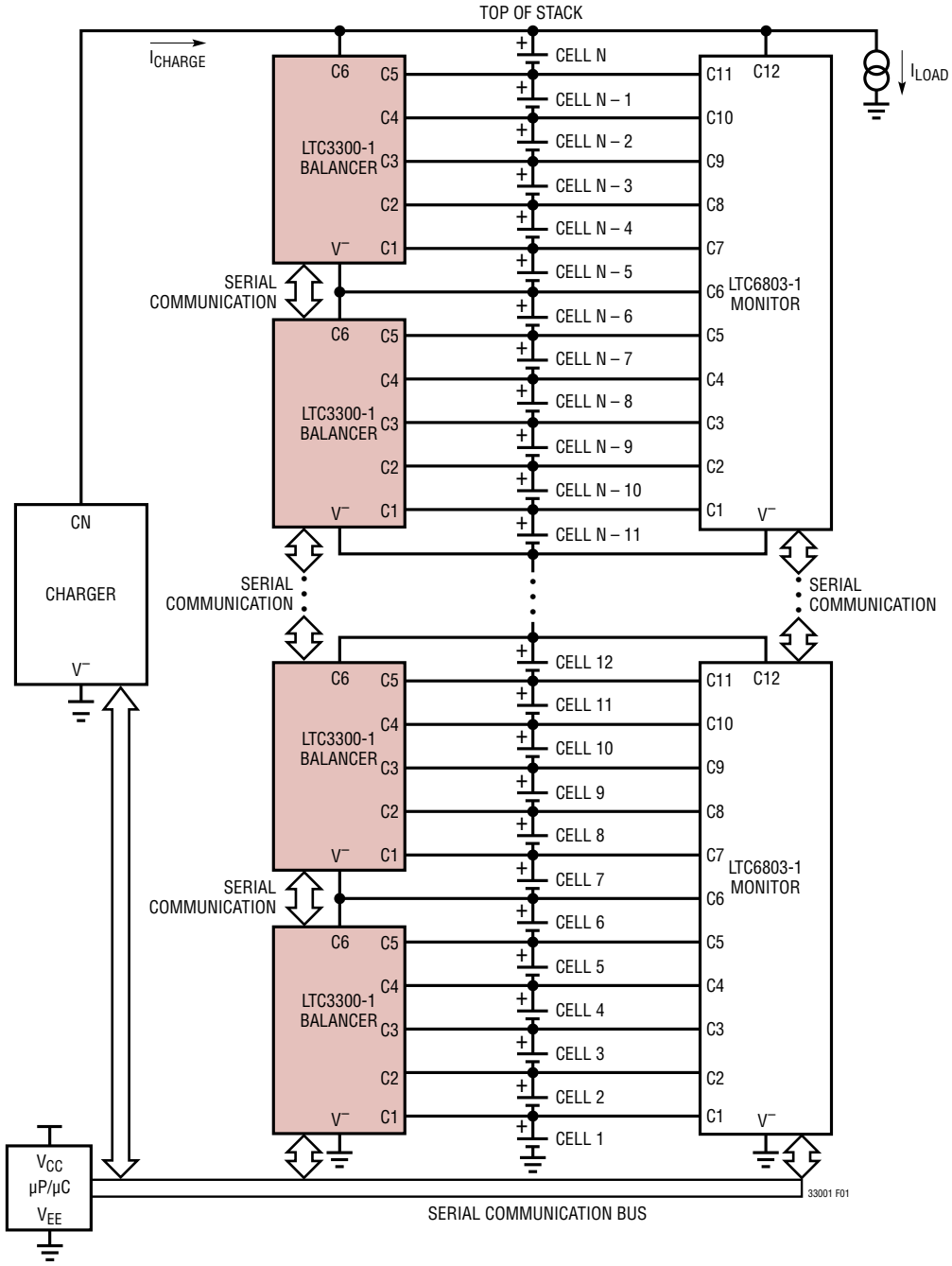


Figure 1. LTC3300-1/LTC6803-1 Typical Battery Management System (BMS)

There is no single balancing algorithm optimal for all situations. For example, during net charging of the overall stack, it may be desirable to discharge the highest voltage cells first to avoid reaching terminal charge on any cell before the entire stack is fully charged. Similarly, during net discharging of the overall stack, it may be desirable to charge the lowest voltage cells first to keep them from reaching a critically low level. Other algorithms may prioritize fastest time to overall balance. The LTC3300-1 implements no algorithm for balancing the stack. Instead it provides maximum flexibility by imposing no limitation on the algorithm implemented as all individual cell balancers can operate simultaneously and bidirectionally.

OPERATION

Unidirectional Versus Bidirectional Balancing

Most balancers in use today employ a unidirectional (discharge only) approach. The simplest of these operate by switching in a resistor across the highest voltage cell(s) in the stack (passive balancing). No charge is recovered in this approach -instead it is dissipated as heat in the resistive element. This can be improved by employing an energy storage element (inductive or capacitive) to transfer charge from the highest voltage cell(s) in the stack to other lower voltage cells in the stack (active balancing). This can be very efficient (in terms of charge recovery) for the case where only a few cells in the overall stack are high, but will be very inefficient (and time consuming) for the case where only a few cells in the overall stack are low. A bidirectional active balancing approach, such as employed by the LTC3300-1, is needed to achieve minimum balancing time and maximum charge recovery for all common cell capacity errors.

Synchronous Flyback Balancer

The balancing architecture implemented by the LTC3300-1 is bidirectional synchronous flyback. Each LTC3300-1 contains six independent synchronous flyback controllers that are capable of directly charging or discharging an individual cell. Balance current is scalable with external components. Each balancer operates independently of the others and provides a means for bidirectional charge transfer between an individual cell and a larger group of adjacent cells. Refer to Figure 2.

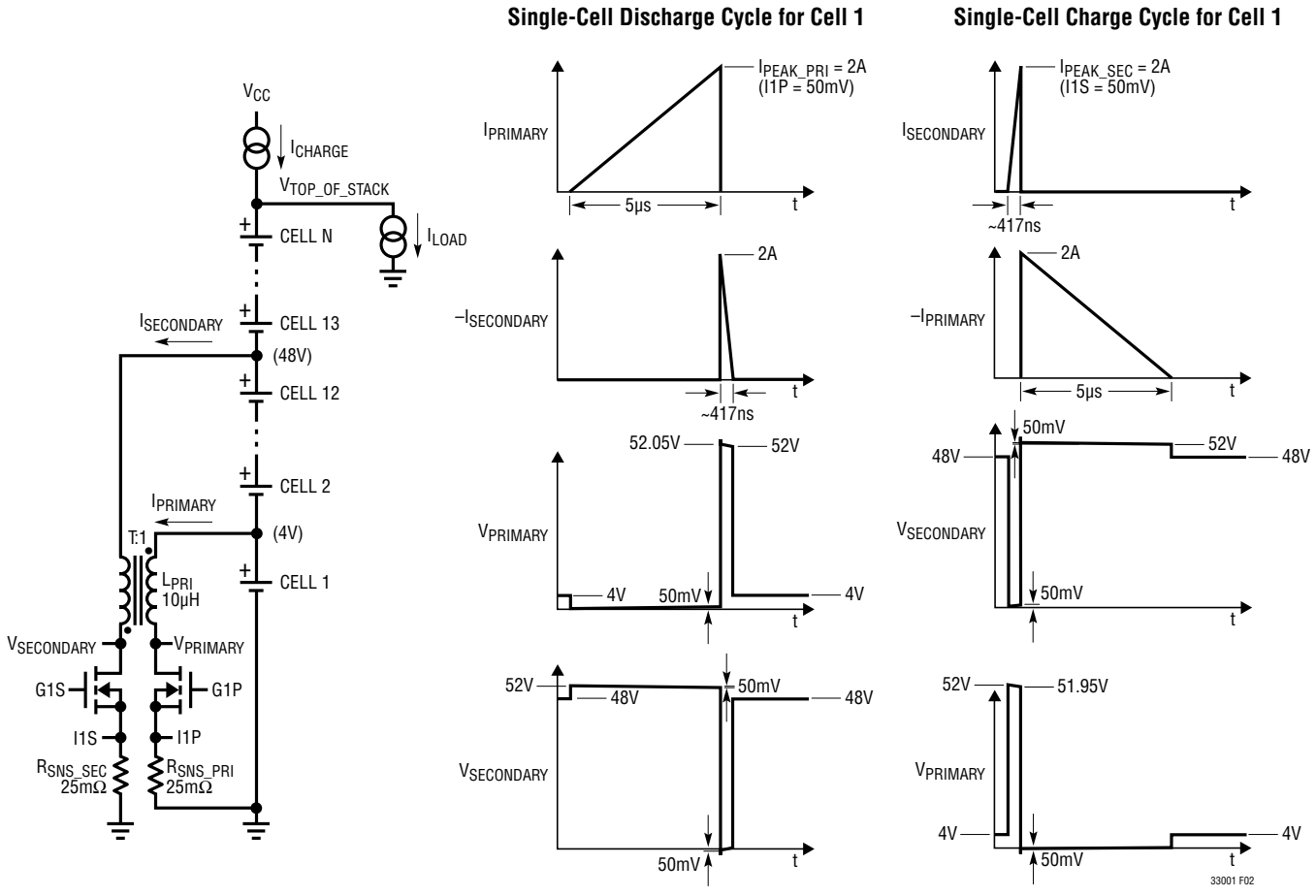


Figure 2. Synchronous Flyback Balancing Example with T = 1, S = 12

OPERATION

Cell Discharging (Synchronous)

When discharging is enabled for a given cell, the primary side switch is turned on and current ramps in the primary winding of the transformer until the programmed peak current (I_{PEAK_PRI}) is detected at the I*n*P pin. The primary side switch is then turned off, and the stored energy in the transformer is transferred to the secondary-side cells causing current to flow in the secondary winding of the transformer. The secondary-side synchronous switch is turned on to minimize power loss during the transfer period until the secondary current drops to zero (detected at I*n*S). Once the secondary current reaches zero, the secondary switch turns off and the primary-side switch is turned back on thus repeating the cycle. In this manner, charge is transferred from the cell being discharged to all of the cells connected between the top and bottom of the secondary side—thereby charging the adjacent cells. In the example of Figure 2, the secondary-side connects across 12 cells including the cell being discharged.

I_{PEAK_PRI} is programmed using the following equation:

$$I_{PEAK\_PRI} = \frac{50mV}{R_{SNS\_PRI}}$$

Cell discharge current (primary side) and secondary-side charge recovery current are determined to first order by the following equations:

$$I_{DISCHARGE} = \frac{I_{PEAK\_PRI}}{2}\left(\frac{S}{S+T}\right)$$

$$I_{SECONDARY} = \frac{I_{PEAK\_PRI}}{2}\left(\frac{1}{S+T}\right)\eta_{DISCHARGE}$$

where S is the number of secondary-side cells, 1:T is the transformer turns ratio from primary to secondary, and $\eta_{DISCHARGE}$ is the transfer efficiency from primary cell discharge to the secondary side stack.

Cell Charging

When charging is enabled for a given cell, the secondary-side switch for the enabled cell is turned on and current flows from the secondary-side cells through the transformer. Once I_{PEAK_SEC} is reached in the secondary side (detected at the I*n*S pin), the secondary switch is turned off and current then flows in the primary side thus charging the selected cell from the entire stack of secondary cells. As with the discharging case, the primary-side synchronous switch is turned on to minimize power loss during the cell charging phase. Once the primary current drops to zero, the primary switch is turned off and the secondary-side switch is turned back on thus repeating the cycle.

I_{PEAK_SEC} is programmed using the following equation:

$$I_{PEAK\_SEC} = \frac{50mV}{R_{SNS\_SEC}}$$

Cell charge current and corresponding secondary-side discharge current are determined to first order by the following equations:

$$I_{CHARGE} = \frac{I_{PEAK\_SEC}}{2}\left(\frac{ST}{S+T}\right)\eta_{CHARGE}$$

$$I_{SECONDARY} = \frac{I_{PEAK\_SEC}}{2}\left(\frac{T}{S+T}\right)$$

where S is the number of secondary cells in the stack, 1:T is the transformer turns ratio from primary to secondary, and η_{CHARGE} is the transfer efficiency from secondary-side stack discharge to the primary-side cell.

Each balancer's charge transfer "frequency" and duty factor depend on a number of factors including I_{PEAK_PRI}, I_{PEAK_SEC}, transformer winding inductances, turns ratio, cell voltage and the number of secondary-side cells.

The frequency of switching seen at the gate driver outputs is given by:

$$f_{DISCHARGE} = \frac{S}{S+T} \bullet \frac{V_{CELL}}{L_{PRI} \bullet I_{PEAK\_PRI}}$$

$$f_{CHARGE} = \frac{S}{S+T} \bullet \frac{V_{CELL}}{L_{PRI} \bullet I_{PEAK\_SEC} \bullet T}$$

where L_{PRI} is the primary winding inductance.

Figure 3 shows a fully populated LTC3300-1 application employing all six balancers.

OPERATION

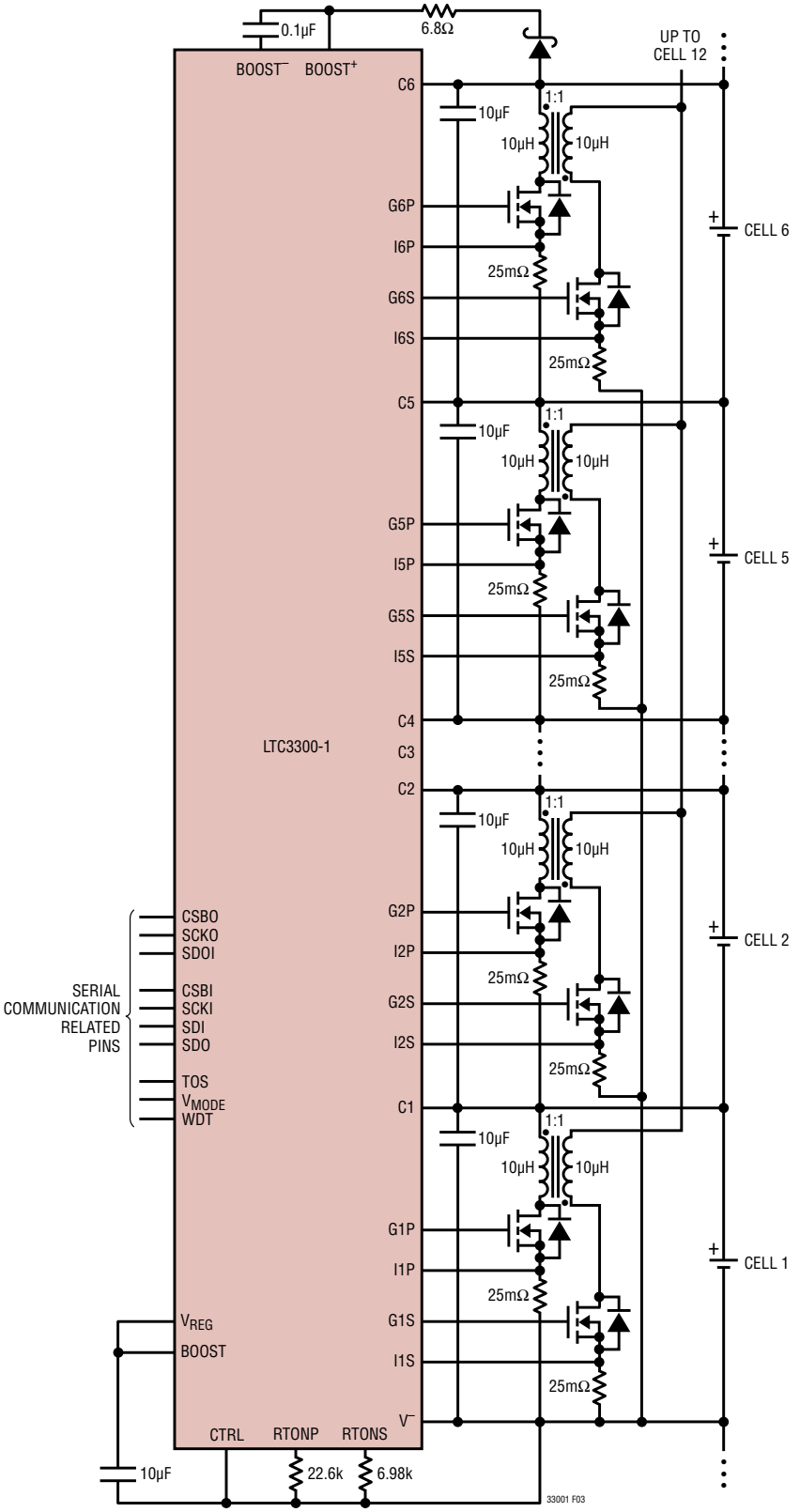


Figure 3. LTC3300-1 6-Cell Active Balancer Module Showing Power Connections for the Multi-Transformer Application (CTRL = V⁻)

OPERATION

Balancing High Voltage Battery Stacks

Balancing series connected batteries which contain >>12 cells in series requires interleaving of the transformer secondary connections in order to achieve full stack balancing while limiting the breakdown voltage requirements of the primary- and secondary-side power FETs. Figure 4 shows typical interleaved transformer connections for a multicell battery stack in the generic sense, and Figure 5 for the specific case of an 18-cell stack. In these examples, the secondary side of each transformer is connected to the top of the cell that is 12 positions higher in the stack than the bottom of the lowest voltage cell in each LTC3300-1 sub-stack. For the top most LTC3300-1 in the stack, it is not possible to connect the secondary side of the transformer across 12 cells. Instead, it is connected to the top of the stack, or effectively across only 6 cells. Interleaving in this fashion allows charge to transfer between 6-cell sub-stacks throughout the entire battery stack.

Max On-Time Volt-Sec Clamps

The LTC3300-1 contains programmable fault protection clamps which limit the amount of time that current is allowed to ramp in either the primary or secondary windings in the event of a shorted sense resistor. Maximum on time for all primary connections (active during cell discharging) and all secondary connections (active during cell charging) is individually programmable by connecting resistors from the R_{TONP} and R_{TONS} pins to V^- according to the following equations:

$$t_{ON(MAX)|PRIMARY} = 7.2\mu s \frac{R_{TONP}}{20k\Omega}$$

$$t_{ON(MAX)|SECONDARY} = 1.2\mu s \frac{R_{TONS}}{15k\Omega}$$

For more information on selecting the appropriate maximum on-times, refer to the Applications Information section.

To defeat this function, short the appropriate R_{TON} pin(s) to V_{REG}.

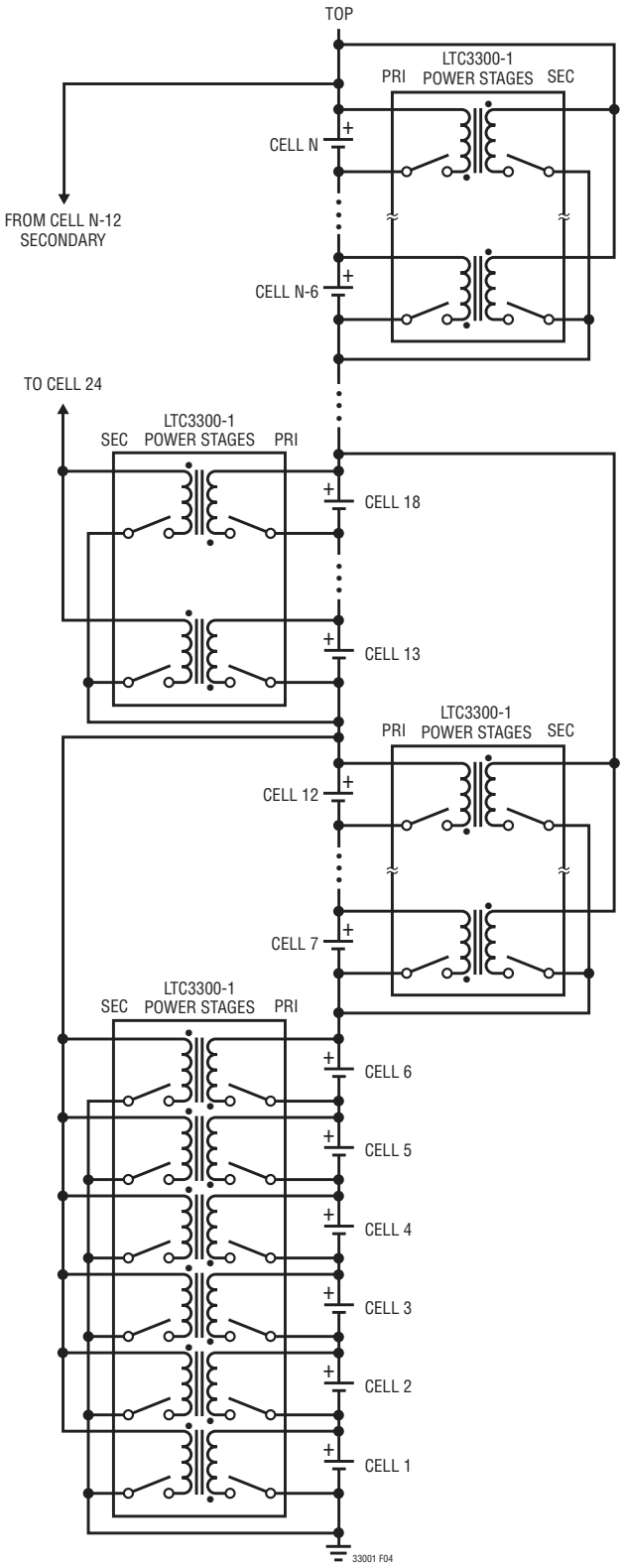


Figure 4. Diagram of Power Transfer Interleaving Through the Stack, Transformer Connections for High Voltage Stacks

OPERATION

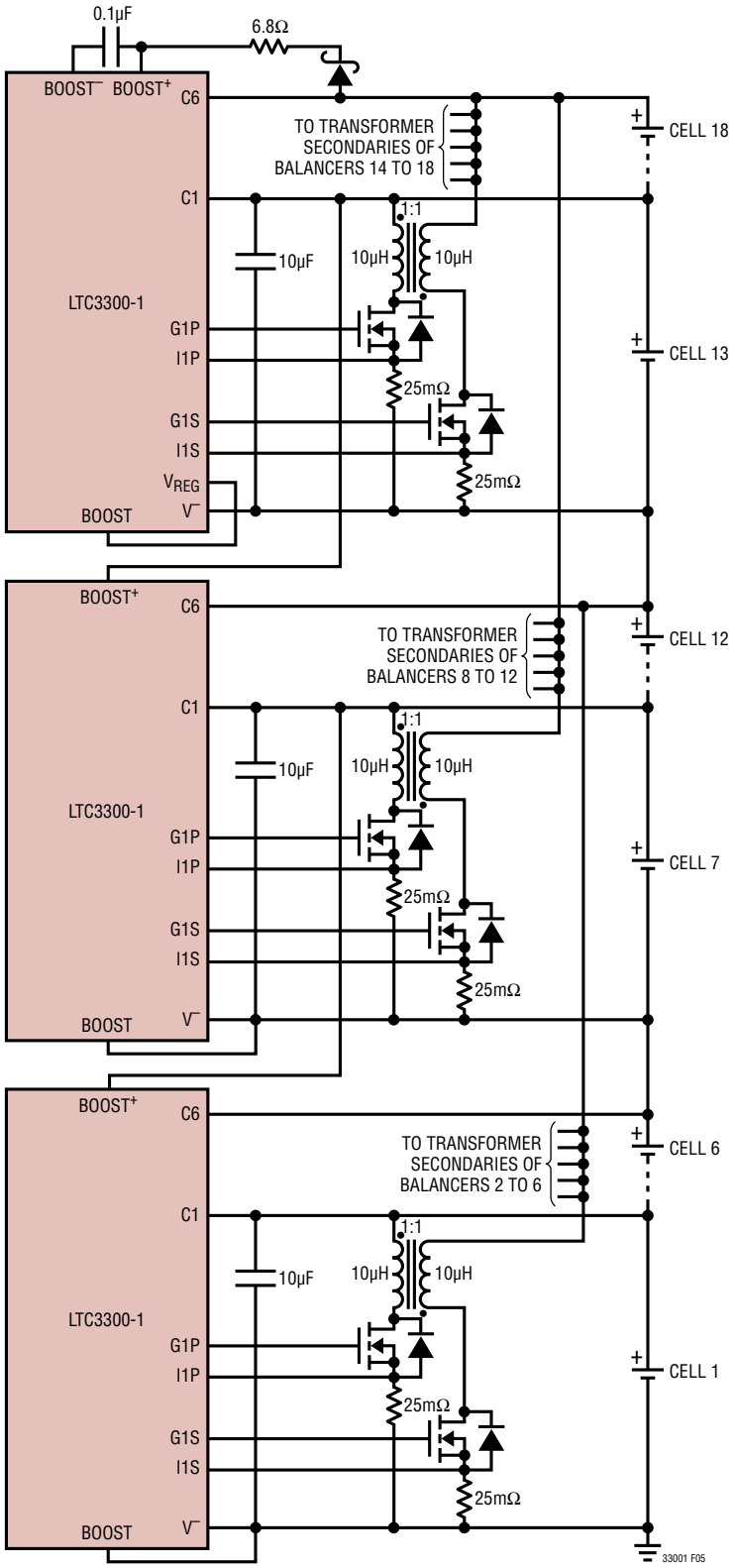


Figure 5. 18-Cell Active Balancer Showing Power Connections, Interleaved Transformer Secondaries and BOOST⁺ Rail Generation Up the Stack

OPERATION

Gate Drivers/Gate Drive Comparators

All secondary-side gate drivers (G1S through G6S) are powered from the V_{REG} output, pulling up to 4.8V when on and pulling down to V^- when off. All primary-side gate drivers (G1P through G6P) are powered from their respective cell voltage and the next cell voltage higher in the stack (see Table 1). An individual cell balancer will only be enabled if its corresponding cell voltage is greater than 2V and the cell voltage of the next higher cell in the stack is also greater than 2V. For the G6P gate driver output, the next higher cell in the stack is C1 of the next higher LTC3300-1 in the stack (if present) and is only used if the boosted gate drive is disabled (by connecting BOOST = V^-). If the boosted gate drive is enabled (by connecting BOOST = V_{REG}), only the C6 cell voltage is looked at to enable balancing of Cell 6. In the case of the topmost LTC3300-1 in the stack, the boosted gate drive must be enabled. The boosted gate drive requires an external diode from C6 to $BOOST^+$ and a boost capacitor from $BOOST^+$ to $BOOST^-$. For information on selecting these components, refer to the Applications Information section. Also note that the dynamic supply current referred to in Note 4 of the Electrical Characteristics table adds to the terminal currents of the pins indicated in the Voltage When Off and Voltage When On columns of Table 1.

The gate drive comparators have a DC hysteresis of 70mV. For improved noise immunity, the inputs are internally low pass filtered and the outputs are filtered so as to not transition unless the internal comparator state is unchanged for 3µs to 6µs (typical). If insufficient gate drive is detected while active balancing is in progress (perhaps, for example, if the stack is under heavy load), the affected balancer(s) and only the affected balancer(s) will shut off. The balance command remains stored in memory, and active balancing will resume where it left off if sufficient gate drive is subsequently restored. This can happen if, for example, the stack is being charged.

Cell Overvoltage Comparators

In addition to sufficient gate drive being required to enable balancing, there are additional comparators which disable all active balancing if any of the six individual cell voltages is greater than 5V. These comparators have a DC hysteresis of 500mV. For improved noise immunity, the inputs are internally low pass filtered and the outputs are filtered so as to not transition unless the internal comparator state is unchanged for 3µs to 6µs (typical). If any cell voltage goes overvoltage while active balancing is in progress, all active balancers will shut off. The balance command remains stored in memory, and active balancing will resume where if left off if the cell voltage subsequently comes back in range. These comparators will protect the LTC3300-1 if a connection to a battery is lost while balancing and the cell voltage is still increasing *as a result of that balancing.*

Table 1

DRIVER OUTPUT	VOLTAGE WHEN OFF	VOLTAGE WHEN ON	GATE DRIVE REQUIRED TO ENABLE BALANCING
G1P	V-	C2	(C2 – C1) ≥ 2V and (C1 – V^-) ≥2V
G2P	C1	C3	(C3 – C2) ≥ 2V and (C2 – C1) ≥2V
G3P	C2	C4	(C4 – C3) ≥ 2V and (C3 – C2) ≥2V
G4P	C3	C5	(C5 – C4) ≥ 2V and (C4 – C3) ≥2V
G5P	C4	C6	(C6 – C5) ≥ 2V and (C5 – C4) ≥2V
G6P	C5	If BOOST = V_{REG}: BOOST+ (Generated)	(C6 – C5) ≥ 2V
		If BOOST = V^-: $BOOST^+$ = C7*	(C7* – C6) ≥ 2V and (C6 – C5) ≥ 2V

*C7 is equal to C1 of the next higher LTC3300-1 in the stack if this connection is used.

OPERATION

Voltage Regulator

A linear voltage regulator powered from C6 creates a 4.8V rail at the V_{REG} pin which is used for powering certain internal circuitry of the LTC3300-1 including all 6 secondary gate drivers. The V_{REG} output can also be used for powering external loads, provided that the total DC loading of the regulator does not exceed 40mA at which point current limit is imposed to limit on-chip power dissipation. The internal component of the DC load current is dominated by the average gate driver current(s) (G1S through G6S), each approximated by C • V • f, where C is the gate capacitance of the external NMOS transistor, V = V_{REG} = 4.8V, and f is the frequency that the gate driver output is running at. FET manufacturers usually specify the C • V product as Q_g (gate charge) measured in coulombs at a given gate drive voltage. The frequency, f, is dependent on many terms, primarily the voltage of each individual cell, the number of cells in the secondary stack, the programmed peak balancing current, and the transformer primary and secondary winding inductances. In a typical application, the C • V • f current loading the V_{REG} output is expected to be low single-digit milliamperes per driver. Note that the V_{REG} loading current is ultimately delivered from the C6 pin. For applications involving very large balance currents and/or employing external NMOS transistors with very large gate capacitance, the V_{REG} output may need to source more than 40mA average. For information on how to design for these situations, refer to the Applications Information section.

One additional function slaved to the V_{REG} output is the power-on reset (POR). During initial power-up and subsequently if the V_{REG} pin voltage ever falls below approximately 4V (e.g., due to overloading), the serial port is cleared to the default power-up state with no balancers active. This feature thus guarantees that the minimum gate drive provided to the external secondary side FETs is also 4V. For a 10µF capacitor loading the output at initial power-up, the output reaches regulation in approximately 1ms.

Thermal Shutdown

The LTC3300-1 has an overtemperature protection circuit which shuts down all active balancing if the internal silicon die temperature rises to approximately 155°C. When in thermal shutdown, all serial communication remains active and the cell balancer status (which contains temperature information) can be read back. The balance command which had been being executed remains stored in memory. This function has 10°C of hysteresis so that when the die temperature subsequently falls to approximately 145°C, active balancing will resume with the previously executing command.

Watchdog Timer Circuit

The watchdog timer circuit provides a means of shutting down all active balancing in the event that communication to the LTC3300-1 is lost. The watchdog timer initiates when a balance command begins executing and is reset to zero every time a valid 8-bit command byte (see Serial Port Operation) is written. The valid command byte can be an execute, a write, or a read (command or status). “Partial” reads and writes are considered valid, i.e., it is only necessary that the first 8 bits have to be written and contain the correct address.

Referring to Figure 6a, at initial power-up and when not balancing, the WDT pin is high impedance and will be pulled high (internally clamped to ~5.6V) if an external pull-up resistor is present. While balancing and during normal communication activity, the WDT pin is pulled low by a precision current source equal to 1.2V/R_{TONS}. (Note: if the secondary volt-second clamp is defeated by connecting R_{TONS} to V_{REG}, the watchdog function is also defeated.) If no valid command byte is written for 1.5 seconds (typical), the WDT output will go back high. When WDT is high, all balancers will be shut down but the previously executing balance command still remains in memory. From this timed-out state, a subsequent valid command byte will reset the timer, but the balancers will

OPERATION

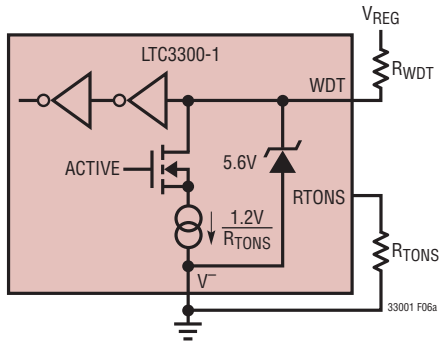
only restart if an execute command is written. To defeat the watchdog function, simply connect the WDT pin to V⁻.

Pause/Resume Balancing (via WDT Pin)

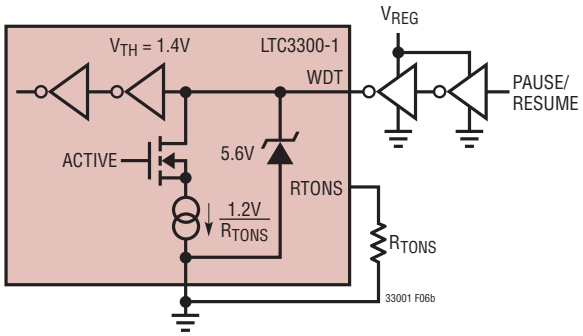
The WDT output pin doubles as a logic input (TTL levels) which can be driven by an external logic gate as shown in Figure 6b (no watchdog), or by a PMOS/three-state logic gate as shown in Figure 6c (with watchdog) to pause and resume balancing in progress. The external pull-up must have sufficient drive capability to override the current source to ground at the WDT pin (=1.2V/R_{TONS}). Provided that the internal watchdog timer has not independently timed out, externally pulling the WDT pin high will immediately pause balancing, and it will resume where it left off when the pin is released.

Secondary Winding OVP Function (via WDT pin)

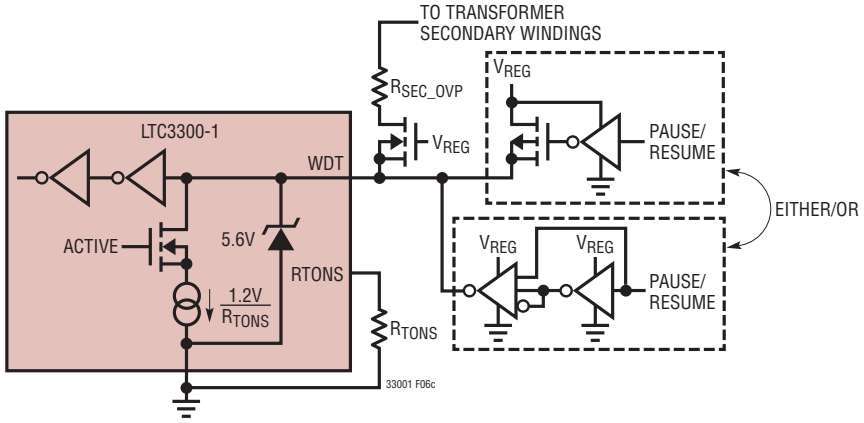
The precision current source pull-down on the WDT pin during balancing can be used to construct an accurate secondary winding OVP protection circuit as shown in Figure 6c. A second external resistor, scaled to R_{TONS} and connected to the transformer secondary winding, is used to set the comparator threshold. An NMOS cascode device (with gate tied to V_{REG}) is also needed to protect



(6a) Watchdog Timer Only (WDT = V⁻ to Defeat)



(6b) Pause/Resume Balancing Only



(6c) Watchdog Timer with Pause/Resume Balancing and Secondary Winding OVP Protection

Figure 6. WDT Pin Connection Options

OPERATION

the WDT pin from high voltage. The secondary winding OVP thresholds are given by:

$V_{SEC|OVP(RISING)} = 1.4V + 1.2V \bullet (R_{SEC\_OVP}/R_{TONS})$

$V_{SEC|OVP(FALLING)} = 1.4V + 1.05V \bullet (R_{SEC\_OVP}/R_{TONS})$

This comparator will protect the LTC3300-1 application circuit if the secondary winding connection to the battery stack is lost while balancing and the secondary winding voltage is still increasing *as a result of that balancing.* The balance command remains stored in memory, and active balancing will resume where it left off if the stack voltage subsequently falls to a safer level.

Single Transformer Application (CTRL = V_{REG})

Figure 7 shows a fully populated LTC3300-1 application employing all six balancers with a single shared custom transformer. In this application, the transformer has six primary windings coupled to a single secondary winding. Only one balancer can be active at a given time as all six share the secondary gate driver G1S and secondary current sense input I1S. The unused gate driver outputs G2S-G6S must be left floating and the unused current sense inputs I2S-I6S should be connected to V^-. Any balance command which attempts to operate more than one balancer at a time will be ignored. This application represents the minimum component count active balancer achievable.

SERIAL PORT OPERATION

Overview

The LTC3300-1 has an SPI bus compatible serial port. Several devices can be daisy chained in series. There are two sets of serial port pins, designated as low side and high side. The low side and high side ports enable devices to be daisy chained even when they operate at different power supply potentials. In a typical configuration, the positive power supply of the first, bottom device is connected to the negative power supply of the second, top device. When devices are stacked in this manner, they can be daisy chained by connecting the high side port of the bottom device to the low side port of the top device. With this arrangement, the master writes to or reads from the cascaded devices as if they formed one long shift register. The LTC3300-1 translates the voltage level of the signals between the low side and high side ports to pass data up and down the battery stack.

Physical Layer

On the LTC3300-1, seven pins comprise the low side and high side ports. The low side pins are CSBI, SCKI, SDI and SDO. The high side pins are CSBO, SCKO and SDOI. CSBI and SCKI are always inputs, driven by the master or by the next lower device in a stack. CSBO and SCKO are always outputs that can drive the next higher device in a stack. SDI is a data input when writing to a stack of devices. For devices not at the bottom of a stack, SDI is a data output when reading from the stack. SDOI is a data output when writing to and a data input when reading from a stack of devices. SDO is an open-drain output that is only used on the bottom device of a stack, where it may be tied with SDI, if desired, to form a single, bidirectional port. The SDO pin on the bottom device of a stack requires a pull-up resistor. For devices up in the stack, SDO should be tied to the local V^- or left floating.

To communicate between daisy-chained devices, the high side port pins of a lower device (CSBO, SCKO and SDOI) should be connected through high voltage diodes to the respective low side port pins of the next higher device (CSBI, SCKI and SDI). In this configuration, the devices communicate using current rather than voltage. To signal a logic high from the lower device to the higher device, the lower device sinks a smaller current from the higher device pin. To signal a logic low, the lower device sinks a larger current. Likewise, to signal a logic high from the higher device to the lower device, the higher device sources a larger current to the lower device pin. To signal a logic low, the higher device sources a smaller current.

OPERATION

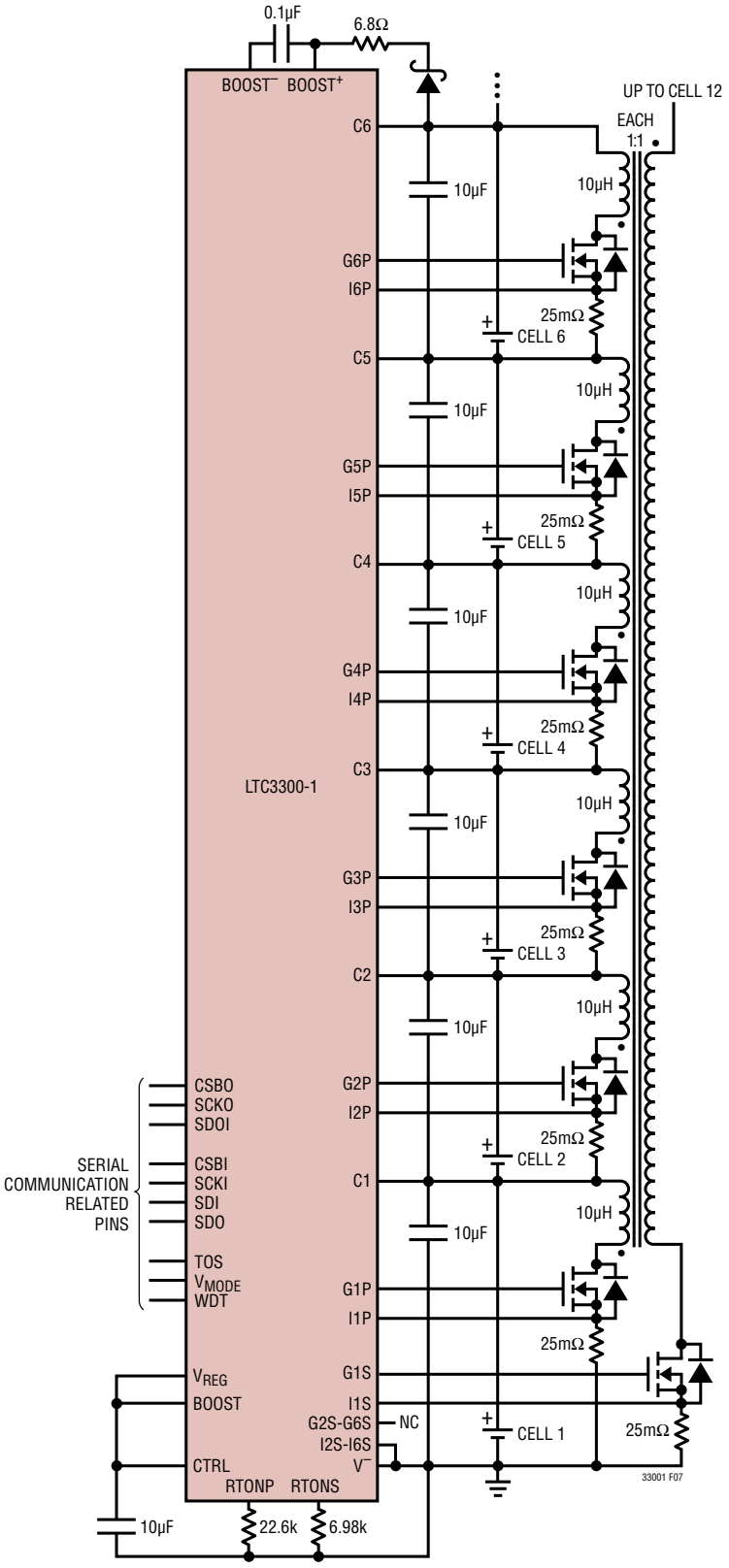


Figure 7. LTC3300-1 6-Cell Active Balancer Module Showing Power Connections For The Single Transformer Application (CTRL = V_{REG})

OPERATION

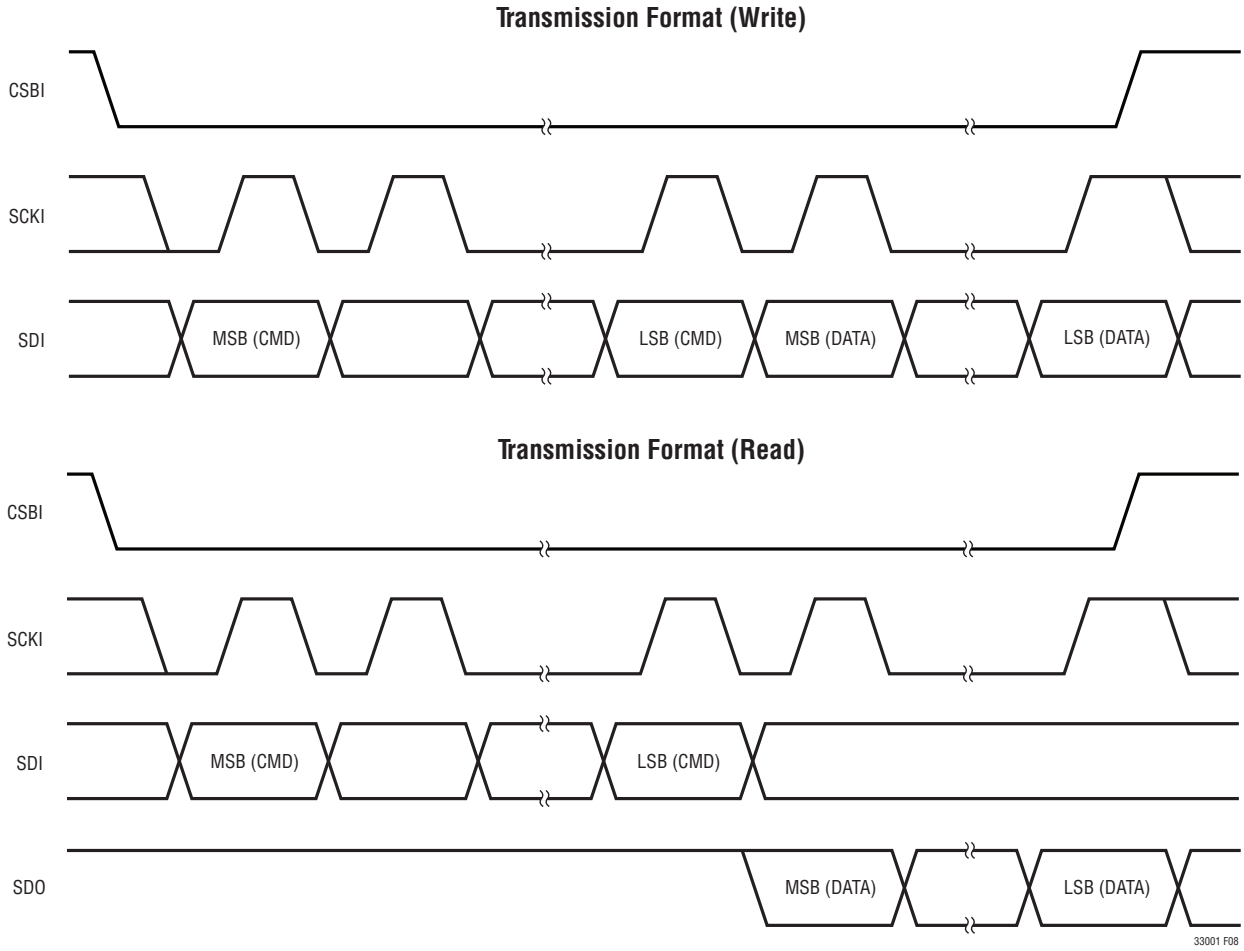


Figure 8

See Figure 9. Since CSBO, SCKO and SDOI voltages are close to the V⁻ of the high side device, the V⁻ of the high side device must be at least 5V higher than that of the low side device to guarantee current flows of the current mode interface. It is recommended that high voltage diodes be placed in series with the SPI daisy-chain signals as shown if Figure 13. These diodes prevent reverse voltage stress on the IC if a battery group bus bar is removed. See Battery Interconnection Integrity for additional information.

Standby current consumed in the current mode serial interface is minimized when CSBI is logic high.

The voltage mode pin (V_{MODE}) determines whether the low side serial port is configured as voltage mode or current mode. For the bottom device in a daisy-chain stack, this

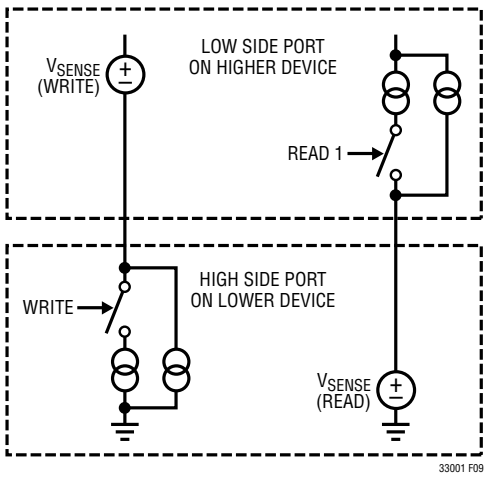


Figure 9. Current Mode Interface

OPERATION

pin must be pulled high (tied to V_{REG}). The other devices in the daisy chain must have this pin pulled low (tied to V^-) to designate current mode communication. To designate the top-of-stack device, the TOS pin on the top device of a daisy chain must be tied high. The other devices in the stack must have TOS tied low. See the application on the last page of this data sheet.

Command Byte

All communication to the LTC3300-1 takes place with CSBI logic low. The first 8 clocked in data bits after a high-to-low transition on CSBI represent the command byte and are level-shifted through all LTC3300-1 ICs in the stack so as to be simultaneously read by all LTC3300-1 ICs in the stack. The 8-bit command byte is written MSB first per Table 2. The first 5 bits must match a fixed internal address [10101] which is common to all LTC3300-1's in the stack, or all subsequent data will be ignored until CSBI transitions high and then low again. The 6th and 7th bits program one of four commands as shown in Table 3. The 8th bit in the command byte must be set such that the entire 8-bit command byte has even parity. If the parity is incorrect, the current balance command being executed (from the last previously successful write) is terminated immediately and all subsequent (write) data is ignored until CSBI transitions high and then low again. Incorrect parity takes this action whether or not the address matches. This thereby provides a fast means to immediately terminate balancing-in-progress by intentionally writing a command byte with incorrect parity.

Table 2. Command Byte Bit Mapping (Defaults to 0x00 in Reset State)

1 (MSB)	0	1	0	1	CMDA	CMDB	Parity Bit (LSB)

Table 3. Command Bits

CMDA	CMDB	Communication Action
0	0	Write Balance Command (without Executing)
0	1	Readback Balance Command
1	0	Read Balance Status
1	1	Execute Balance Command

Write Balance Command

If the command bits program Write Balance Command, all subsequent write data must be mod 16 bits (before CSBI transitions high) or it will be ignored. The internal command holding register will be cleared which can be verified on readback. The current balance command being executed (from the last previously successful write) will continue, but all active balancing will be turned off if an Execute Balance Command is subsequently written. Each LTC3300-1 in the stack expects 16 bits of write data written MSB first per Table 4. Successive 16-bit write data is shifted in starting with the highest LTC3300-1 in the stack and proceeding down the stack. In this manner, the first 16 bits will be the write data for the topmost LTC3300-1 in the stack and will have shifted through all other LTC3300-1 ICs in the stack. The last 16 bits will be the write data for the bottom-most LTC3300-1 in the stack.

Table 4. Write Balance Command Data Bit Mapping (Defaults to 0x000F in Reset State)

D1A (MSB)	D1B	D2A	D2B	D3A	D3B	D4A	D4B	D5A	D5B	D6A	D6B	$\overline{CRC[3]}$	$\overline{CRC[2]}$	$\overline{CRC[1]}$	$\overline{CRC[0]}$ (LSB)

OPERATION

The first 12 bits of the 16-bit balance command are used to indicate which balancer (or balancers) is active and in which direction (charge or discharge). Each of the 6 cell balancers is controlled by 2 bits of this data per Table 5. The balancing algorithm for a given cell is:

Charge Cell *n*: Ramp up to I_{PEAK} in secondary winding, ramp down to I_{ZERO} in primary winding. Repeat.

Discharge Cell *n* (Synchronous): Ramp up to Ipeak in primary winding, ramp down to I_{ZERO} in secondary winding. Repeat.

Table 5. Cell Balancer Control Bits

D*n*A	D*n*B	Balancing Action (*n* = 1 to 6)
0	0	None
0	1	Discharge Cell *n* (Nonsynchronous)
1	0	Discharge Cell *n* (Synchronous)
1	1	Charge Cell *n*

For nonsynchronous discharging of cell *n*, both the secondary winding gate drive and (zero) current sense amp are disabled. The secondary current will conduct either through the body diode of the secondary switch (if present) or through a substitute Schottky diode. The primary will only turn on again after the secondary winding Volt-sec clamp times out. In a bidirectional application with a secondary switch, it may be possible to achieve slightly higher discharge efficiency by opting for nonsynchronous discharge mode (if the gate charge savings exceed the added diode drop losses) but the balancing current will be less predictable because the secondary winding Volt-sec clamp must be set longer than the expected time for the current to hit zero in order to guarantee no current reversal. In the case where a Schottky diode replaces the secondary switch, it is possible to build a undirectional discharge-only balancing application charging an isolated auxiliary cell as shown in Figure 19 in the Typical Applications section.

In the CTRL = 1 application of Figure 7 employing a single transformer which can only balance one cell at a time, any command requesting simultaneous balancing of more than one cell will be ignored. All active balancing will be turned off if an Execute Balance Command is subsequently written.

The last 4 bits of the 16-bit balance command are used for packet error checking (PEC). The 16 bits of write data (12-bit message plus 4-bit CRC) are input to a cyclic redundancy check (CRC) block employing the International Telecommunication Union CRC-4 standard characteristic polynomial:

$x^4 + x + 1$

In the write data, the 4-bit CRC appended to the message must be selected such that the remainder of the CRC division is zero. *Note that the CRC bits in the Write Balance Command are inverted.* This was done so that an "all zeros" command is invalid. The LTC3300-1 will ignore the write data if the remainder is not zero and the internal command holding register will be cleared which can be verified on readback. The current balance command being executed (from the last previously successful write) will continue, but all active balancing will be turned off if an Execute Balance Command is subsequently written. For information on how to calculate the CRC including an example, refer to the Applications Information section.

Readback Balance Command

The bit mapping for Readback Balance Command is identical to that for Write Balance Command. If the command bits program Readback Balance Command, successive 16-bit previously written data (latched in 12-bit message plus newly calculated 4-bit CRC) are shifted out in the same order bitwise (MSB first) starting with the lowest LTC3300-1 in the stack and proceeding up the stack. Thus, the sequence of outcoming data during readback is:

Command data (bottom chip), Command data (2nd chip from bottom), …, Command data (top chip)

This command allows for microprocessor verification of written commands before executing. *Note that the CRC bits in the Readback Balance Command are also inverted*. This was done so that an "all zeros" readback is invalid.

OPERATION

Read Balance Status

If the command bits program Read Balance Status, successive 16-bit status data (12 bits of data plus associated 4-bit CRC) are shifted out MSB first per Table 6. Similar to a Readback Balance Command, the last 4 bits in each 16-bit balance status are used for error detection. The first 12 bits of the status are input to a cyclic redundancy check (CRC) block employing the same characteristic polynomial used for write commands. The LTC3300-1 will calculate and append the appropriate 4-bit CRC to the outgoing 12-bit message which can then be used for microprocessor error checking. The sequence of outcoming data during readback is:

Status data (bottom chip), Status data (2nd chip from bottom), …, Status data (top chip)

Note that the CRC bits in the Read Balance Status are inverted. This was done so that an "all zeros" readback is invalid.

The first 6 bits of the read balance status indicate if there is sufficient gate drive for each of the 6 balancers. These bits correspond to the right-most column in Table 1, but can only be logic high for a given balancer following an execute command involving that same balancer. If a balancer is not active, its Gate Drive OK bit will be logic low. The 7th, 8th, and 9th bits in the read balance status indicate that all 6 cells are not overvoltage, that the transformer secondary is not overvoltage, and that the LTC3300-1 die is not overtemperature, respectively. These 3 bits can only be logic high following an execute command involving at least one balancer. The 10th, 11th, and 12th bits in the read balance status are currently not used and will always be logic zero. As an example, if balancers 1 and 4 are both active with no voltage or temperature faults, the 12-bit read balance status should be 100100111000.

Execute Balance Command

If the command bits program Execute Balance Command, the last successfully written and latched in balance command will be executed immediately. All subsequent (write) data will be ignored until CSBI transitions high and then low again.

Pause/Resume Balancing (via SPI Port)

The LTC3300-1 provides a simple means to interrupt balancing in progress (stack wide) and then restart without having to rewrite the previous balance command to all LTC3300-1 ICs in the stack. To pause balancing, simply write an 8-bit Execute Balance Command with the parity bit flipped: 10101110. To resume balancing, simply write an Execute Balance Command with the correct parity: 10101111. This feature is useful if precision cell voltage measurements want to be performed during balancing with the stack "quiet." Immediate pausing of balancing in progress will occur for *any* 8-bit Command Byte with incorrect parity.

The restart time is typically 2ms which is the same as the delayed start time after a new or different balance command (t_{DLY_START}). It is measured from the 8th rising SCKI edge until the balancer turns on and is illustrated in G27 in the Typical Performance Characteristics section.

Table 6. Read Balance Status Data Bit Mapping (defaults to 0x000F in Reset State)

Gate Drive 1 OK (MSB)	Gate Drive 2 OK	Gate Drive 3 OK	Gate Drive 4 OK	Gate Drive 5 OK	Gate Drive 6 OK	Cells Not OV	Sec Not OV	Temp OK	0	0	0	$\overline{CRC[3]}$	$\overline{CRC[2]}$	$\overline{CRC[1]}$	$\overline{CRC[0]}$ (LSB)

APPLICATIONS INFORMATION

External Sense Resistor Selection

The external current sense resistors for both primary and secondary windings set the peak balancing current according to the following formulas:

$$R_{SENSE|PRIMARY} = \frac{50mV}{I_{PEAK\_PRI}}$$

$$R_{SENSE|SECONDARY} = \frac{50mV}{I_{PEAK\_SEC}}$$

Balancer Synchronization

Due to the stacked configuration of the individual synchronous flyback power circuits and the interleaved nature of the gate drivers, it is possible at higher balance currents for adjacent and/or penadjacent balancers within a group of six to sync up. The synchronization will typically be to the highest frequency of any active individual balancer and can result in a slightly *lower* balance current in the other affected balancer(s). This error will typically be very small provided that the individual cells are not significantly out of balance voltage-wise and due to the matched I_{PEAK}/I_{ZERO}'s and matched power circuits. Balancer synchronization can be reduced by lowpass filtering the primary and/or secondary current sense signals with a simple RC network as shown in Figure 10. A good starting point for the RC time constant is one-tenth of the on-time of the associated switch (primary or secondary). In the case of I_{PEAK} sensing, phase lag associated with the lowpass filter will result in a slightly lower voltage seen by the

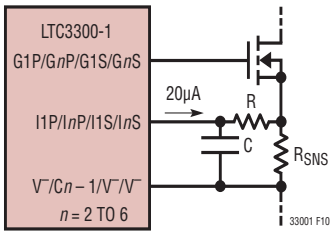


Figure 10. Using an RC Network to Filter Current Sense Inputs to the LTC3300-1

LTC3300-1 compared to the true sense resistor voltage. This error can be compensated for by selecting the R value to add back this same drop using the typical current value of 20µA out of the LTC3300-1 current sense pins at the comparator trip point.

Setting Appropriate Max On-Times

The primary and secondary winding volt-second clamps are intended to be used as a current runaway protection feature and not as a substitute means of current control replacing the sense resistors. In order to not interfere with normal I_{PEAK}/I_{ZERO} operation, the maximum on times must be set longer than the time required to ramp to I_{PEAK} (or I_{ZERO}) for the minimum cell voltage seen in the application:

$$t_{ON(MAX)|PRIMARY} > L_{PRI} \bullet I_{PEAK\_PRI}/V_{CELL(MIN)}$$

$$t_{ON(MAX)|SECONDARY} > L_{PRI} \bullet I_{PEAK\_SEC} \bullet T/(S \bullet V_{CELL(MIN)})$$

These can be further increased by 20% to account for manufacturing tolerance in the transformer winding inductance and by 10% to account for I_{PEAK} variation.

APPLICATIONS INFORMATION

External FET Selection

In addition to being rated to handle the peak balancing current, external NMOS transistors for both primary and secondary windings must be rated with a drain-to-source breakdown such that for the primary MOSFET:

$$V_{DS(BREAKDOWN)|MIN} > V_{CELL} + \frac{V_{STACK} + V_{DIODE}}{T}$$

$$= V_{CELL}\left(1 + \frac{S}{T}\right) + \frac{V_{DIODE}}{T}$$

and for the secondary MOSFET:

$$V_{DS(BREAKDOWN)|MIN} > V_{STACK} + T\left(V_{CELL} + V_{DIODE}\right)$$

$$= V_{CELL}\left(S + T\right) + T\,V_{DIODE}$$

where S is the number of cells in the secondary winding stack and 1:T is the transformer turns ratio from primary to secondary. For example, if there are 12 Li-Ion cells in the secondary stack and using a turns ratio of 1:2, the primary FETs would have to be rated for greater than 4.2V (1 + 6) + 0.5 = 29.9V and the secondary FETs would have to be rated for greater than 4.2V (12 + 2) + 2V = 60.8V.

Good design practice recommends increasing this voltage rating by at least 20% to account for higher voltages present due to leakage inductance ringing. See Table 7 for a list of FETs that are recommended for use with the LTC3300-1.

Table 7

PART NUMBER	MANUFACTURER	$I_{DS(MAX)}$	$V_{DS(MAX)}$
SiR882DP	Vishay	60A	100V
SiS892DN	Vishay	25A	100V
IPD70N10S3-12	Infineon	70A	100V
IPB35N10S3L-26	Infineon	35A	100V
RJK1051DPB	Renesas	60A	100V
RJK1054DPB	Renesas	92A	100V

Transformer Selection

The LTC3300-1 is optimized to work with simple 2-winding transformers with a primary winding inductance of between 1 and 20 microhenries, a 1:2 turns ratio (primary to secondary), and the secondary winding paralleling up to 12 cells. If a larger number of cells in the secondary stack is desired for more efficient balancing, a transformer with a higher turns ratio can be selected. For example, a 1:10 transformer would be optimized for up to 60 cells in the secondary stack. In this case the external FETs would need to be rated for a higher voltage (see above). In all cases the saturation current of the transformer must be selected to be higher than the peak currents seen in the application.

See Table 8 for a list of transformers that are recommended for use with the LTC3300-1.

Table 8

PART NUMBER	MANUFACTURER	TURNS RATIO*	PRIMARY INDUCTANCE	I_{SAT}
750312504 (SMT)	Würth Electronics	1:1	3.5µH	10A
750312667 (THT)	Würth Electronics	1:1	3.5µH	10A
MA5421-AL	Coilcraft	1:1	3.4µH	10A
CTX02-18892-R	Coiltronics	1:1	3.4µH	10A
XF0036-EP135	XFMRS Inc	1:1	3µH	10A
LOO-321	BH Electronics	1:1	3.4µH	10A
DHCP-X79-1001	TOKO	1:1	3.4µH	10A
C128057LF	GCI	1:1	3.4µH	10A
T10857-1	Inter Tech	1:1	3.4µH	10A

*All transformers listed in the table are 8-pin components and can be configured with turns ratios of 1:1, 1:2, 2:1, or 2:2.

Snubber Design

Careful attention must be paid to any transient ringing seen at the drain voltages of the primary and secondary winding FETs in application. The peak of the ringing should not approach and must not exceed the breakdown voltage rating of the FETs chosen. Minimizing leakage inductance present in the application and utilizing good board layout techniques can help mitigate the amount of ringing. In some applications, it may be necessary to place a series resistor + capacitor snubber network in parallel with each winding of the transformer. This network will typically lower efficiency by a few percent, but will keep the FETs in a safer operating region. Determining values for R and C usually requires some trial-and-error optimization in the application. For the transformers shown in Table 8, good starting point values for the snubber network are 330Ω in series with 100pF.

APPLICATIONS INFORMATION

Boosted Gate Drive Component Selection (BOOST = V_{REG})

The external boost capacitor connected from BOOST+ to BOOST– supplies the gate drive voltage required for turning on the external NMOS connected to G6P. This capacitor is charged through the external Schottky diode from C6 to BOOST+ when the NMOS is off (G6P = BOOST– = C5). When the NMOS is to be turned on, the BOOST– driver switches the lower plate of the capacitor from C5 to C6, and the BOOST+ voltage common modes up to one cell voltage higher than C6. When the NMOS turns off again, the BOOST– driver switches the lower plate of the capacitor back to C5 so that the boost capacitor is refreshed.

A good rule of thumb is to make the value of the boost capacitor 100 times that of the input capacitance of the NMOS at G6P. For most applications, a 0.1µF/10V capacitor will suffice. The reverse breakdown of the Schottky diode must only be greater than 6V. To prevent an excessive and potentially damaging surge current from flowing in the boosted gate drive components during initial connection of the battery voltages to the LTC3300-1, it is recommended to place a 6.8Ω resistor in series with the Schottky diode as shown in Figure 3. The surge current must be limited to 1A to avoid potential damage.

Sizing the Cell Bypass Caps for Broken Connection Protection

If a single connection to the battery stack is lost while balancing, the differential cell voltages seen by the LTC3300-1 power circuit on each side of the break can increase or decrease depending on whether charging or discharging and where the actual break occurred. The worst-case scenario is when the balancers on each side of the break are both active and balancing in opposite directions. In this scenario, the differential cell voltage will increase rapidly on one side of the break and decrease rapidly on the other. The cell overvoltage comparators working in conjunction with appropriately-sized differential cell bypass capacitors protect the LTC3300-1 and its associated power components by shutting off all balancing before any local differential cell voltage reaches its absolute maximum rating. The comparator threshold (rising) is 5V, and it takes 3µs to 6µs for the balancing to stop, during which the bypass capacitor must prevent the differential cell voltage from increasing past 6V. Therefore, the minimum differential bypass capacitor value for full broken connection protection is:

$$C_{BYPASS(MIN)} = \frac{(I_{CHARGE} + I_{DISCHARGE}) \bullet 6\mu s}{6V - 5V}$$

If I_{CHARGE} and $I_{DISCHARGE}$ are set nominally equal, then approximately 12µF of real capacitance per amp of balance current is required.

Protection from a broken connection to a cluster of secondary windings is provided local to each LTC3300-1 in the stack by the secondary winding OVP function (via WDT pin) described in the Operation section. However, because of the interleaving of the transformer windings up the stack, it is possible for a remote LTC3300-1 to still act on the cell voltage seen locally by another LTC3300-1 at the point of the break which has shut itself off. For this reason, each cluster of secondary windings must have a dedicated connection to the stack separate from the individual cell connection that it connects to.

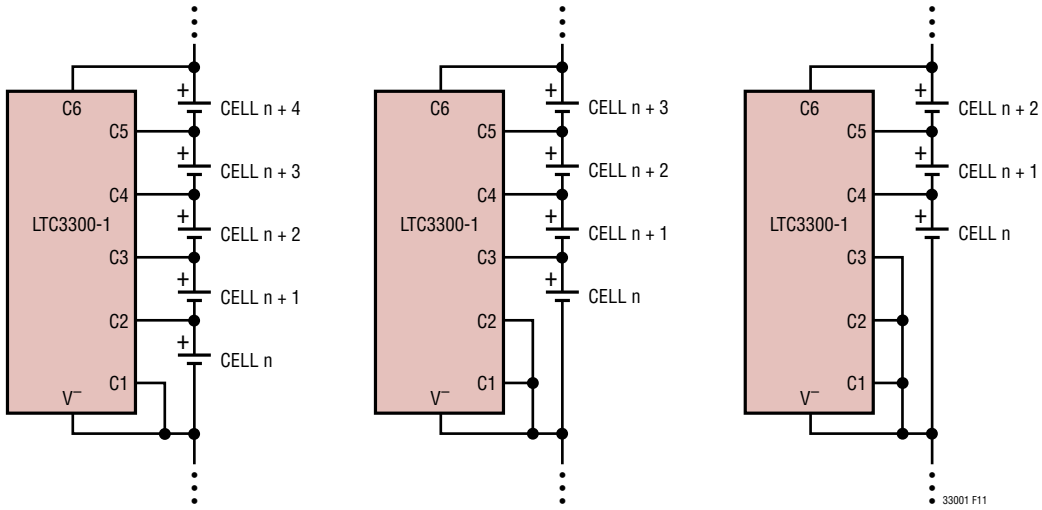
Using the LTC3300-1 with Fewer Than 6 Cells

To balance a series stack of N cells, the required number of LTC3300-1 ICs is N/6 rounded up to the nearest integer. Additionally, each LTC3300-1 in the stack must interface to a minimum of 3 cells (must include C4, C5, and C6). Thus, any stack of 3 or more cells can be balanced using an appropriate stack of LTC3300-1 ICs. Unused cell inputs (C1, C1 + C2, or C1 + C2 + C3) in a given LTC3300 -1 sub-stack should be shorted to V– (see Figure 11). However, in all configurations, the write data remains at 16 bits. The LTC3300-1 will not act on the cell balancing bits for the unused cell(s) but these bits are still included in the CRC calculation.

Supplementary Voltage Regulator Drive (>40mA)

The 4.8V linear voltage regulator internal to the LTC3300-1 is capable of providing 40mA at the V_{REG} pin. If additional current capability is required, the V_{REG} pin can be back-driven by an external low cost 5V buck DC/DC regulator powered from C6 as shown in Figure 12. The internal regulator of the LTC3300-1 has very limited sink current capability and will not fight the higher forced voltage.

APPLICATIONS INFORMATION



(11a) Sub-Stack Using Only 5 Cells **(11b) Sub-Stack Using Only 4 Cells** **(11c) Sub-Stack Using Only 3 Cells**

Figure 11. Battery Stack Connections For 5, 4 or 3 Cells

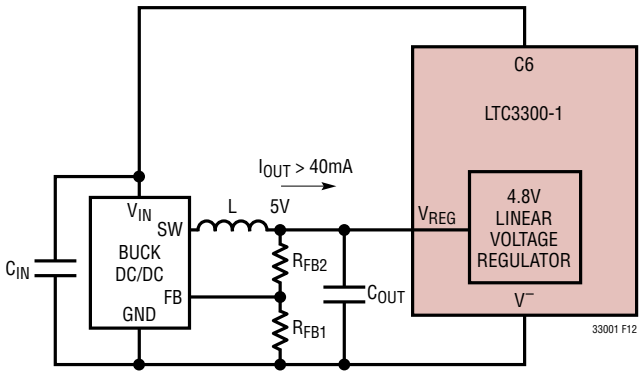


Figure 12. Adding External Buck DC/DC for >40mA V_{REG} Drive

APPLICATIONS INFORMATION

Fault Protection

Care should always be taken when using high energy sources such as batteries. There are numerous ways that systems can be misconfigured when considering the assembly and service procedures that might affect a battery system during its useful lifespan. Table 9 shows the various situations that should be considered when planning protection circuitry. The first four scenarios are to be anticipated during production and appropriate protection is included within the LTC3300-1 device itself.

Table 9. LTC3300-1 Failure Mechanism Effect Analysis

SCENARIO	EFFECT	DESIGN MITIGATION
Top cell (C6) input connection loss to LTC3300-1.	Power will come from highest connected cell input or via data port fault current.	Clamp diodes at each pin to C6 and V^- (within IC) provide alternate power path. Diode conduction at data ports will impair communication with higher potential units.
Bottom cell (V^-) input connection loss to LTC3300-1.	Power will come from lowest connected cell input or via data port fault current.	Clamp diodes at each pin to C6 and V^- (within IC) provide alternate power path. Diode conduction at data ports will impair communication with higher potential units.
Random cell (C1-C5) input connection loss to LTC3300-1.	Power-up sequence at IC inputs/differential input voltage overstress.	Clamp diodes at each pin to C6 and V^- (within IC) provide alternate power path. Zener diodes across each cell voltage input pair (within IC) limit stress.
Disconnection of a harness between a sub-stack of battery cells and the LTC3300-1 (in a system of stacked groups).	Loss of all supply connections to the IC.	Clamp diodes at each pin to C6 and V^- (within IC) provide alternate power path if there are other devices (which can supply power) connected to the LTC3300-1. Diode conduction at data ports will impair communication with higher potential units.
Secondary winding connection loss to battery stack.	Secondary winding power FET could be subjected to a higher voltage as bypass capacitor charges up.	WDT pin implements a secondary winding OVP circuit which will detect overvoltage and terminate balancing.
Shorted primary winding sense resistor.	Primary winding peak current cannot be detected to shut off primary switch.	Maximum ON-time set by R_{TONP} resistor will shut off primary switch if peak current detect doesn't occur.
Shorted secondary winding sense resistor.	Secondary winding peak current cannot be detected to shut off secondary switch.	Maximum ON-time set by R_{TONS} resistor will shut off secondary switch if peak current detect doesn't occur.
Data link disconnection between stacked LTC3300-1 units.	Break of daisy-chain communication (no stress to ICs). Communication will be lost to devices above the disconnection. The devices below the disconnection are still able to communicate and perform all functions.	If the watchdog timer is enabled, all balancers above the fault will be turned off after 1.5 seconds. The individual WDT pins will go Hi-Z and be pulled up by external resistors.
Data error (noise margin induced or otherwise) occurs during a write command.	Incoming checksum will not agree with the incoming message when read in by any individual LTC3300-1 in the stack.	Since the CRC remainder will not be zero, the LTC3300-1 will not execute the write command, even if an execute command is given. All balancers with nonzero remainders will be off.
Data error (noise margin induced or otherwise) occurs during a read command.	Outgoing checksum (calculated by the LTC3300-1) will not agree with the outgoing message when read in by the host microprocessor.	Since the CRC remainder (calculated by the host) will not be zero, the data cannot be trusted. All balancers will remain in the state of the last previously successful write.

APPLICATIONS INFORMATION

Battery Interconnection Integrity

The FMEA scenarios involving a break in the stack of battery cells are potentially the most damaging. In the case where the battery stack has a discontinuity between groupings of cells balanced by LTC3300-1 ICs, any load will force a large reverse potential on the daisy-chain connection. This situation might occur in a modular battery system during initial installation or a service procedure. The daisy-chain ports are protected from the reverse potential in this scenario by external series high voltage diodes required in the upper port data connections as shown in Figure 13.

During the charging phase of operation, this fault would lead to forward biasing of daisy-chain ESD clamps that would also lead to part damage. An alternative connection to carry current during this scenario will avoid this stress from being applied (Figure 13).

Internal Protection Diodes

Each pin of the LTC3300-1 has protection diodes to help prevent damage to the internal device structures caused by external application of voltages beyond the supply rails as shown in Figure 14. The diodes shown are conventional silicon diodes with a forward breakdown voltage of 0.5V. The unlabeled Zener diode structures have a reverse-breakdown characteristic which initially breaks down at 9V then snaps back to a 7V clamping potential. The Zener diodes labeled Z_{CLAMP} are higher voltage devices with an initial reverse breakdown of 25V snapping back to 22V. The forward voltage drop of all Zeners is 0.5V.

The internal protection diodes shown in Figure 14 are power devices which are intended to protect against limited-power transient voltage excursions. Given that these voltages exceed the absolute maximum ratings of the LTC3300-1, any sustained operation at these voltage levels *will* damage the IC.

Initial Battery Connection to LTC3300-1

In addition to the above-mentioned internal protection diodes, there are additional lower voltage/lower current diodes across each of the six differential cell inputs (not shown in Figure 14) which protect the LTC3300-1 during initial installation of the battery voltages in the application. These diodes have a breakdown voltage of 5.3V with 20kΩ of series resistance and keep the differential cell voltages below their absolute maximum rating during power-up when the cell terminal currents are zero to tens of microamps. This allows the six batteries to be connected in any random sequence without fear of an unconnected cell input pin overvoltaging due to leakage currents acting on its high impedance input. Differential cell-to-cell bypass capacitors used in the application must be of the same nominal value for full random sequence protection.

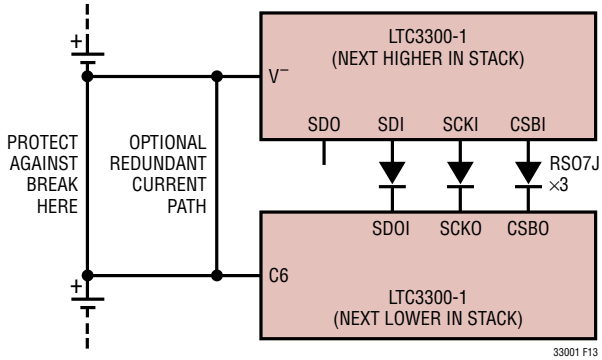


Figure 13. Reverse-Voltage Protection for the Daisy Chain (One Link Connection Shown)

APPLICATIONS INFORMATION

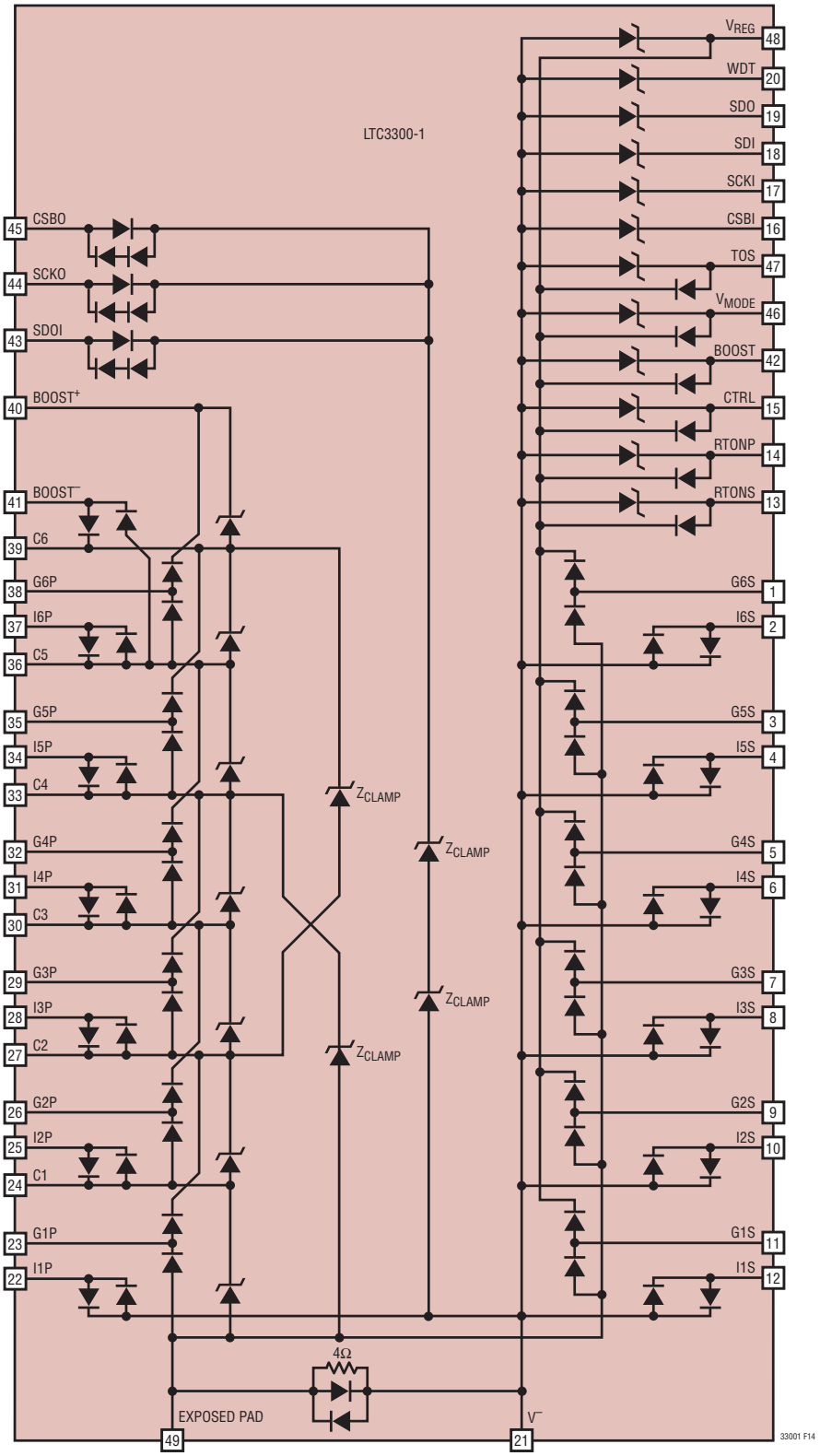


Figure 14. Internal Protection Diodes

APPLICATIONS INFORMATION

Analysis of Stack Terminal Currents in Shutdown

As given in the Electrical Characteristics table, the quiescent current of the LTC3300-1 when not balancing is 16µA at the C6 pin and zero at the C1 through C5 pins. All of this 16µA shows up at the V^- pin of the LTC3300-1. In addition, the SPI port when not communicating (i.e., CSBI = 1) contributes an additional 2.5µA per high side line (CSBO/SCKO/SDOI), or 7.5µA to the V^- pin current of each LTC3300-1 in the stack which is not top of stack (TOS = 0). This additional current does not add to the local C6 pin current but rather to the C6 pin current *of the next higher* LTC3300-1 in the stack as it is passed in through the CSBI/SCKI/SDI pins. To the extent that the 16µA and 7.5µA currents match perfectly chip-to-chip in a long series stack, the resultant stack terminal currents in shutdown are as follows: 23.5µA out of the top of stack node, 7.5µA out of the node 6 cells below top of stack, 7.5µA into the node 6 cells above bottom of stack, and 23.5µA into the bottom of stack node. All other intermediate node currents are zero. This is shown graphically in Figure 15. For the specific case of a 12-cell stack, this reduces to only 23.5µA out of the top of stack node and 23.5µA into the bottom of stack node.

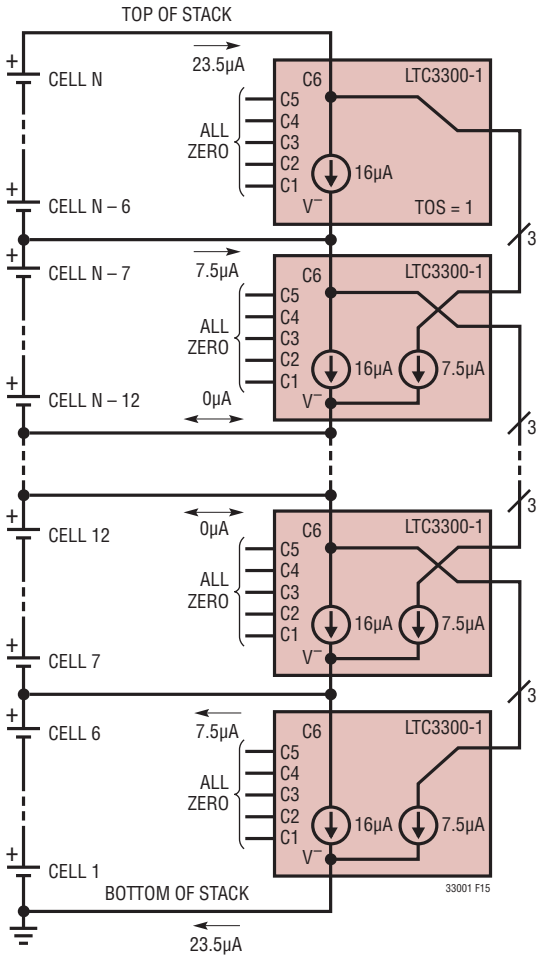


Figure 15. Stack Terminal Currents in Shutdown

APPLICATIONS INFORMATION

How to Calculate the CRC

One simple method of computing an n-bit CRC is to perform arithmetic modulo-2 division of the n+1 bit characteristic polynomial into the m bit message appended with n zeros (m+n bits). Arithmetic modulo-2 division resembles normal long division absent borrows and carries. At each intermediate step of the long division, if the leading bit of the dividend is a 1, a 1 is entered in the quotient and the dividend is exclusive-ORed bitwise with the divisor. If the leading bit of the dividend is a 0, a 0 is entered in the quotient and the dividend is exclusive-ORed bitwise with n zeros. This process is repeated m times. At the end of the long division, the quotient is disregarded and the n-bit remainder is the CRC. This will be more clear in the example to follow.

For the CRC implementation in the LTC3300-1, n = 4 and m = 12. The characteristic polynomial employed is $x^4 + x + 1$, which is shorthand for $1x^4 + 0x^3 + 0x^2 + 1x^1 + 1x^0$, resulting in 10011 for the divisor. The message is the first 12 bits of the balance command. Suppose for example the desired balance command calls for simultaneous charging of Cell 1 and synchronous discharging of Cell 4. The 12-bit message (MSB first) will be 110000010000. Appending 4 zeros results in 1100000100000000 for the dividend. The long division is shown in Figure 16a with a resultant CRC of 1101. Note that the CRC bits in the write balance command are inverted. Thus the correct 16-bit balance command is 1100000100000010. Figure 16b shows the same long division procedure being used to check the CRC of data (command or status) read back from the LTC3300-1. In this scenario, the remainder after the long division must be zero (0000) for the data to be valid. Note that the readback CRC bits must be inverted in the dividend before performing the division.

An alternate method to calculate the CRC is shown in Figure 17 in which the balance command bits are input to a combinational logic circuit comprised solely of 2-input exclusive-OR gates. This “brute force” implementation is easily replicated in a few lines of C code.

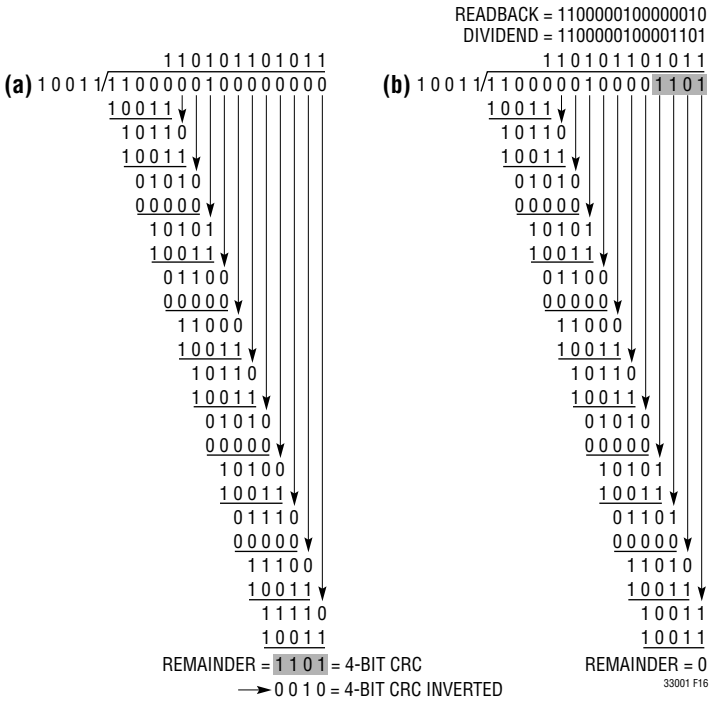


Figure 16. (a) Long Division Example to Calculate CRC for Writes. (b) Long Division Example to Check CRC for Reads

APPLICATIONS INFORMATION

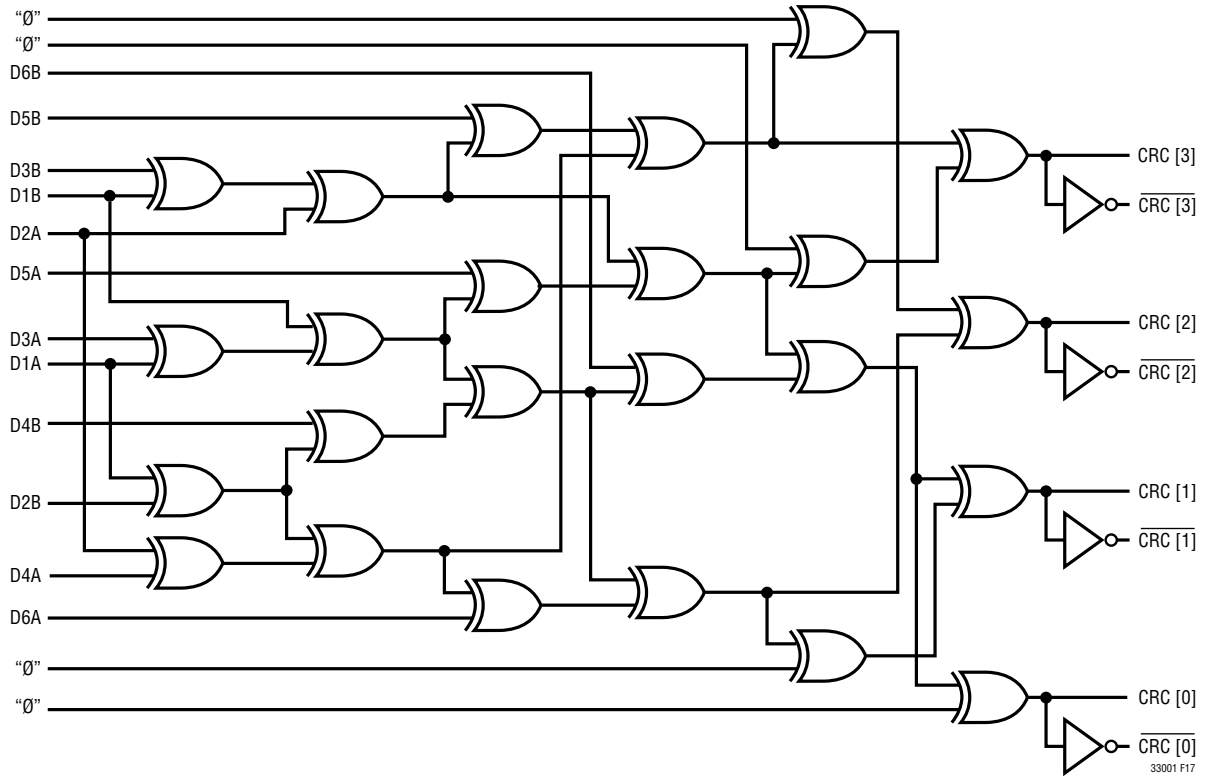


Figure 17. Combinational Logic Circuit Implementation of The CRC Calculator

Serial Communication Using the LTC6803 and LTC6804

The LTC3300-1 is compatible with and convenient to use with all LTC monitor chips, such as the LTC6803 and LTC6804. Figure 20 in the Typical Applications section shows the serial communications connections for a joint LTC3300-1/LTC6803-1 BMS using a common microprocessor SPI port. The SCKI, SDI, and SDO lines of the lowermost LTC3300-1 and LTC6803-1 are tied together. The CSBI lines, however, must be separated to prevent talking to both ICs at the same time. This is easily accomplished by using one of the GPIO outputs from the LTC6803-1 to gate and invert the CSBI line to the LTC3300-1. In this setup, communicating to the LTC6803-1 is no different than without the LTC3300-1, as the GPIO1 output bit is normally high. To talk to the LTC3300-1, written commands must be "bookended" with a GPIO1 negation write to the LTC6803-1 prior to talking to the LTC3300-1 and with a GPIO1 assertion write after talking to the LTC3300-1. Communication "up the stack" passes between LTC3300-1 ICs and between LTC6803-1 ICs as shown.

The Typical Application shown on the back page of this data sheet shows the serial communication connections for a joint LTC3300-1/LTC6804-1 BMS. Each stacked 12-cell module contains two LTC3300-1 ICs and a single LTC6804-1 monitor IC. The upper LTC3300-1 in each module is configured with V_{MODE} = 0, TOS = 1, and receives its serial communication from the lower LTC3300-1 in the same module, which itself is configured with V_{MODE} = 1, TOS = 0. The LTC6804-1 in the same module is configured to provide an effective SPI port output at its GPIO3, GPIO4, and GPIO5 pins which connect directly to the low side communication pins (CSBI, SDI=SDO, SCKI) of the lower LTC3300-1. Communication to the lowermost LTC6804-1 and between monitor chips is done via the LTC6820 and the isoSPI™ interface. In this application, unused battery cells can be shorted from the bottom of any module (i.e., outside the module, not on the module board) as shown without any decrease in monitor accuracy.

APPLICATIONS INFORMATION

PCB Layout Considerations

The LTC3300-1 is capable of operation with as much as 40V between BOOST+ and V–. Care should be taken on the PCB layout to maintain physical separation of traces at different potentials. The pinout of the LTC3300-1 was chosen to facilitate this physical separation. There is no more than 8.4V between any two adjacent pins with the exception of two instances (V_{MODE} to CSBO, BOOST to SDOI/BOOST–). In both instances, one of the pins (V_{MODE}, BOOST) is pin-strapped in the application to V– or V_{REG} and does not need to route far from the LTC3300-1. The package body is used to separate the highest voltage (e.g., 25.2V) from the lowest voltage (0V). As an example, Figure 18 shows the DC voltage on each pin with respect to V– when six 4.2V battery cells are connected to the LTC3300-1.

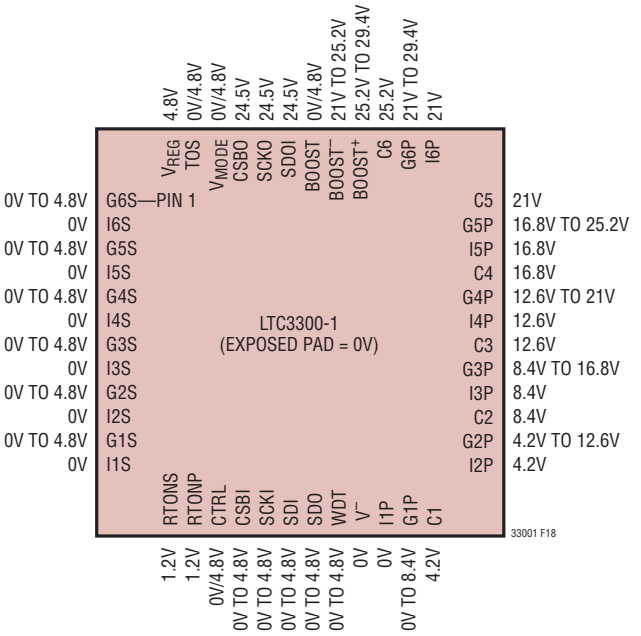


Figure 18. Typical Pin Voltages for Six 4.2V Cells

Additional "good practice" layout considerations are as follows:

1. The V_{REG} pin should be bypassed to the exposed pad and to V–, each with 1µF or larger capacitors as close to the LTC3300-1 as possible.
2. The differential cell inputs (C6 to C5, C5 to C4, …, C1 to exposed pad) should be bypassed with a 1µF or larger capacitor as close to the LTC3300-1 as possible. This is in addition to bulk capacitance present in the power stages.
3. Pin 21 (V–) is the ground sense for current sense resistors connected to I1S-I6S and I1P (seven resistors). Pin 21 should be Kelvined as well as possible with low impedance traces to the ground side of these resistors *before* connecting to the LTC3300-1 exposed pad.
4. Cell inputs C1 to C5 are the ground sense for current sense resistors connected to I2P-I6P (five resistors). These pins should be Kelvined as well as possible with low impedance traces to the ground side of these resistors.
5. The ground side of the maximum on-time setting resistors connected to the RTONS and RTONP pins should be Kelvined to Pin 21 (V–) *before* connecting to the LTC3300-1 exposed pad.
6. Trace lengths from the LTC3300-1 gate drive outputs (G1S-G6S and G1P-G6P) and current sense inputs (I1S-I6S and I1P-I6P) should be as short as possible.
7. The boosted gate drive components (diode and capacitor), if used, should form a tight loop close to the LTC3300-1 C6, BOOST+, and BOOST– pins.
8. For the external power components (transformer, FETs and current sense resistors), it is important to keep the area encircled by the two high speed current switching loops (primary and secondary) as tight as possible. This is greatly aided by having two additional bypass capacitors local to the power circuit: one differential cell to cell and one from the transformer secondary to local V–.

A representative layout incorporating all of these recommendations is implemented on the DC2064A demo board for the LTC3300-1 (with further explanation in its accompanying demo board manual). PCB layout files (.GRB) are also available from the factory.

TYPICAL APPLICATIONS

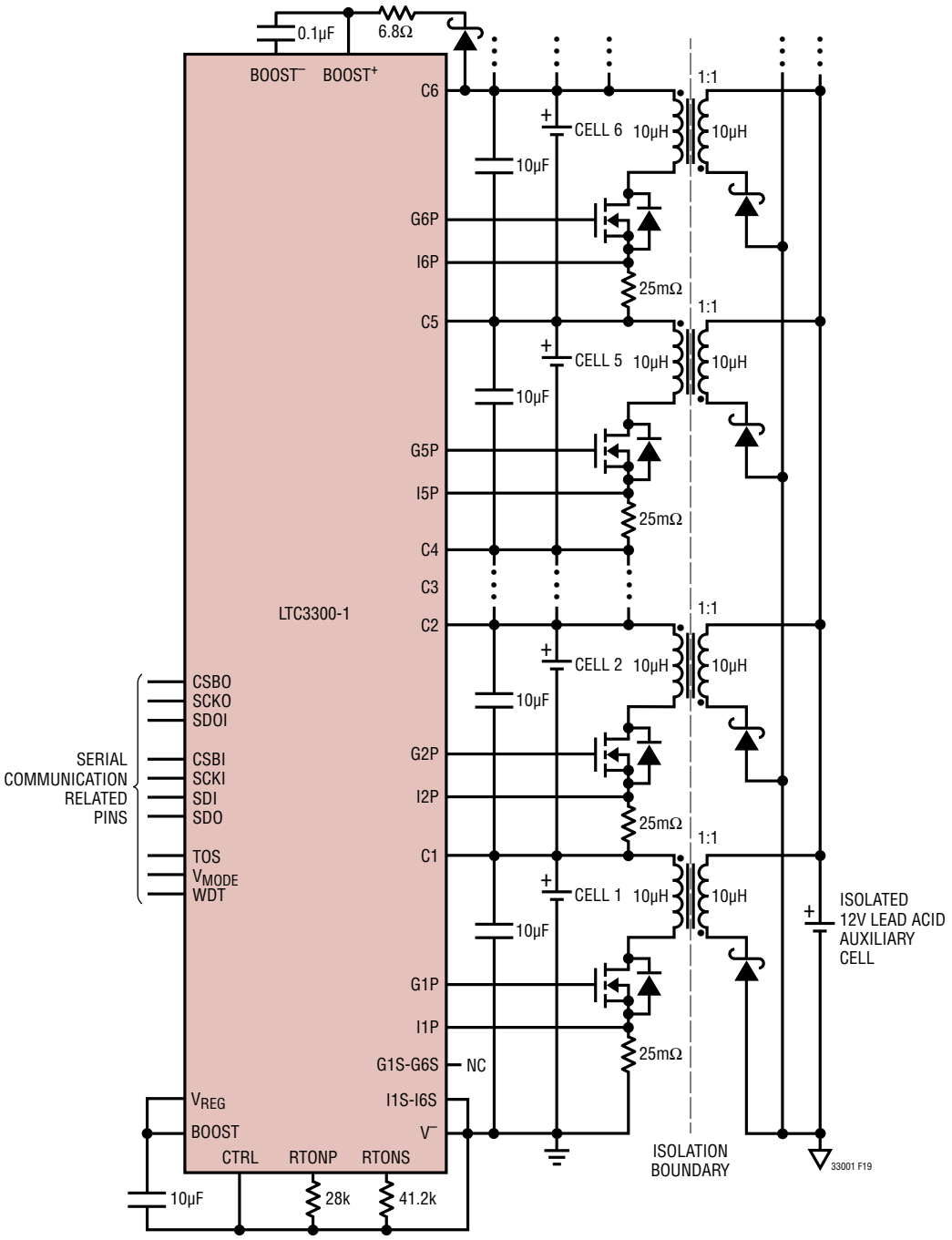


Figure 19. LTC3300-1 Unidirectional Discharge-Only Balancing Application to Charge an Isolated Auxiliary Cell

TYPICAL APPLICATIONS

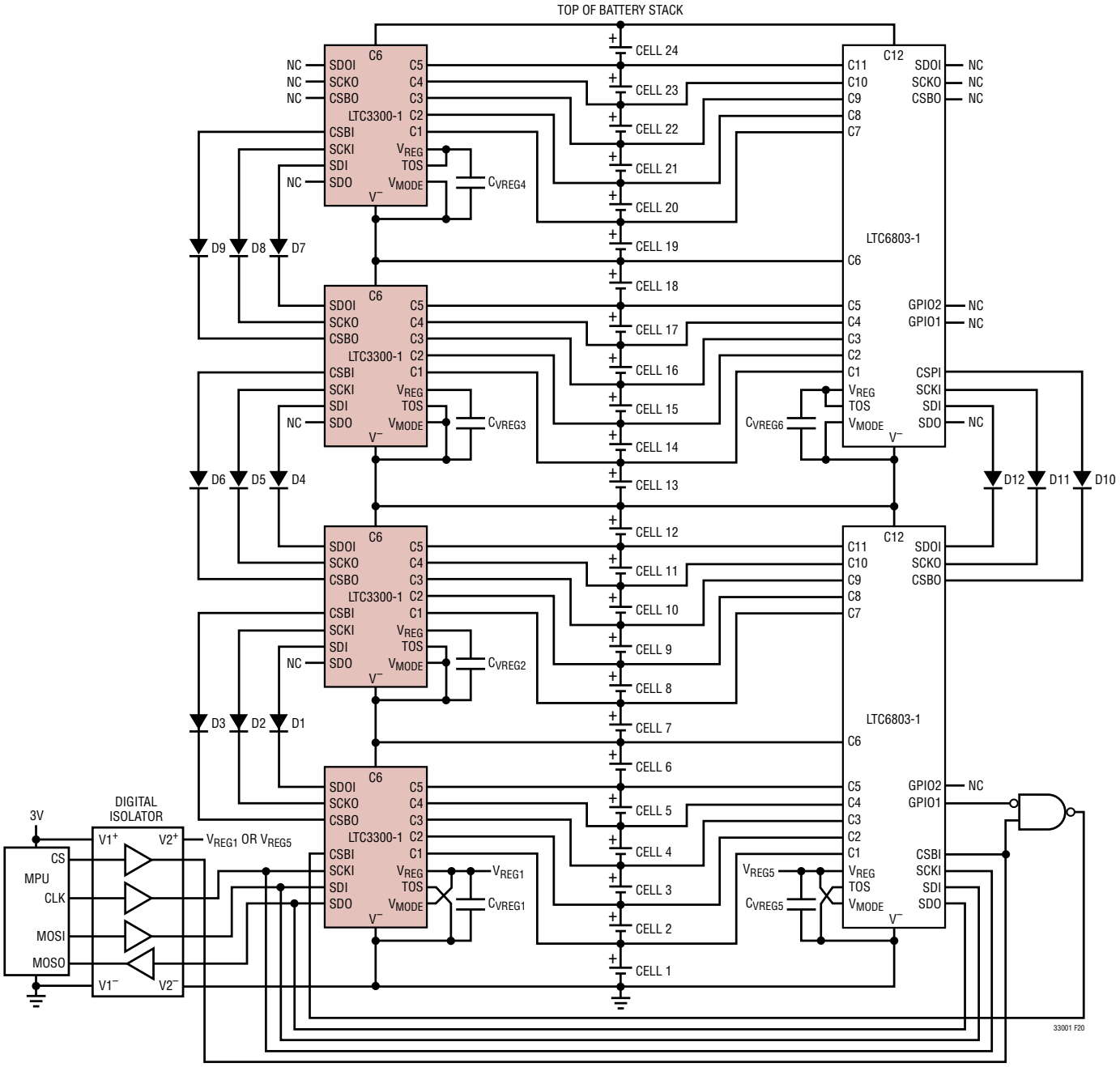
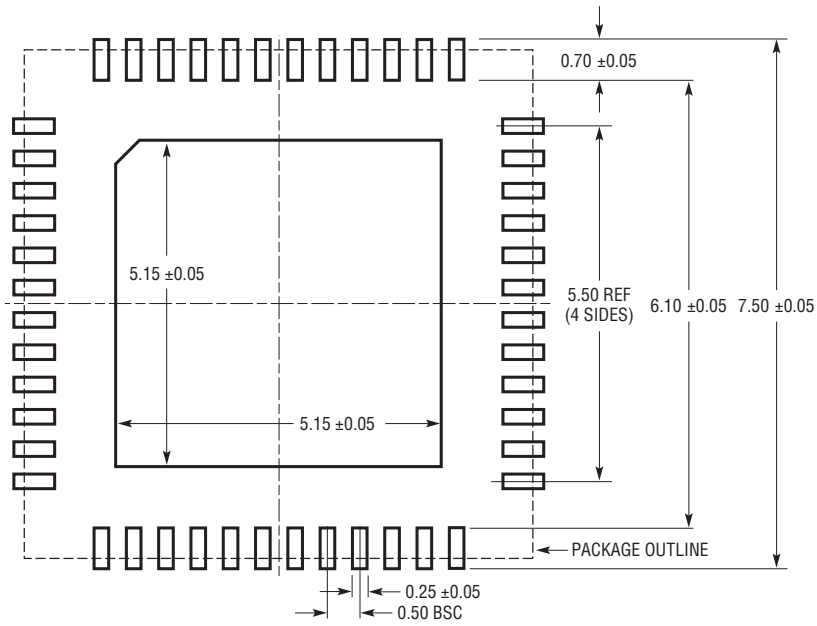


Figure 20. LTC3300-1/LTC6803-1 Battery and Serial Communication Connections for a 24-Cell Stack

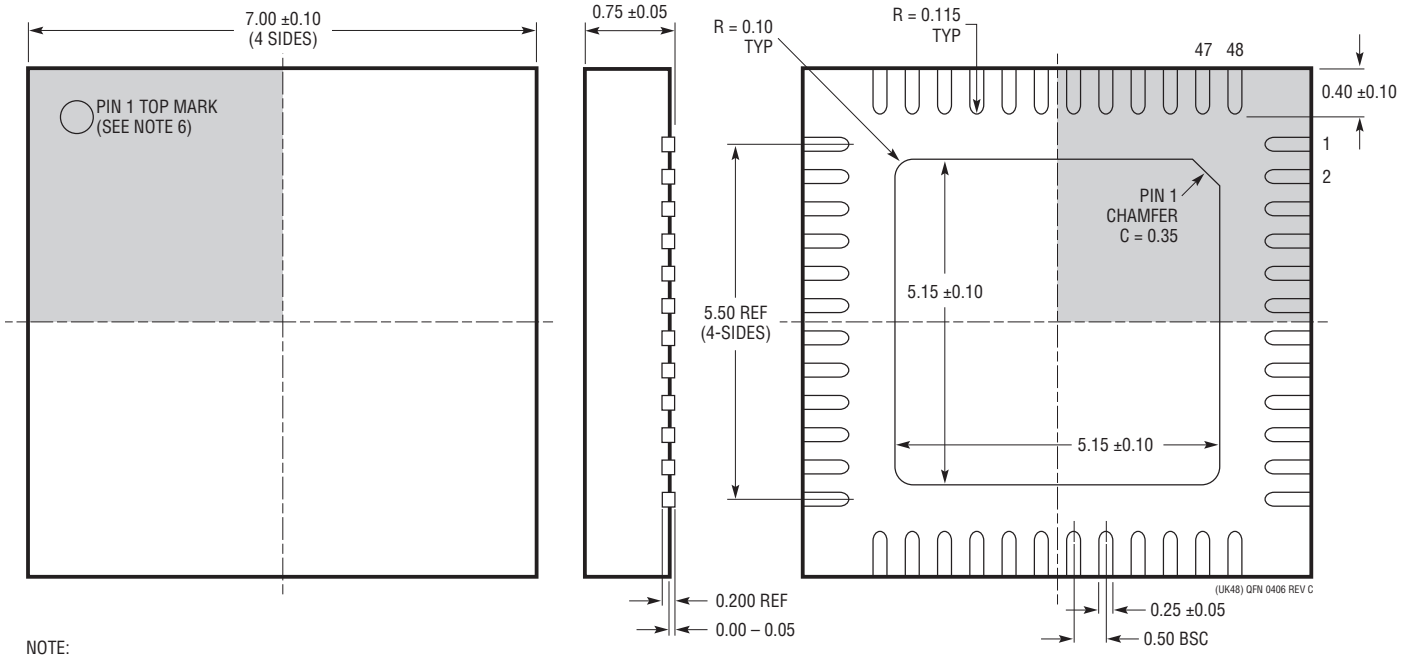
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UK Package
48-Lead Plastic QFN (7mm × 7mm)
(Reference LTC DWG # 05-08-1704 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



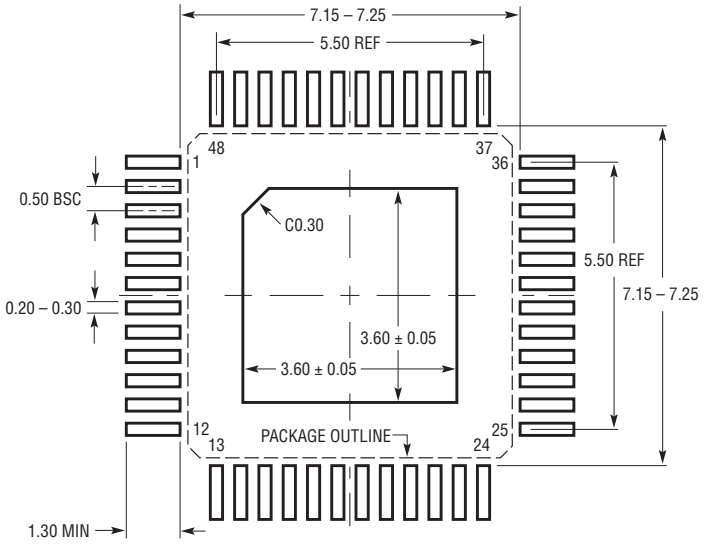
BOTTOM VIEW—EXPOSED PAD

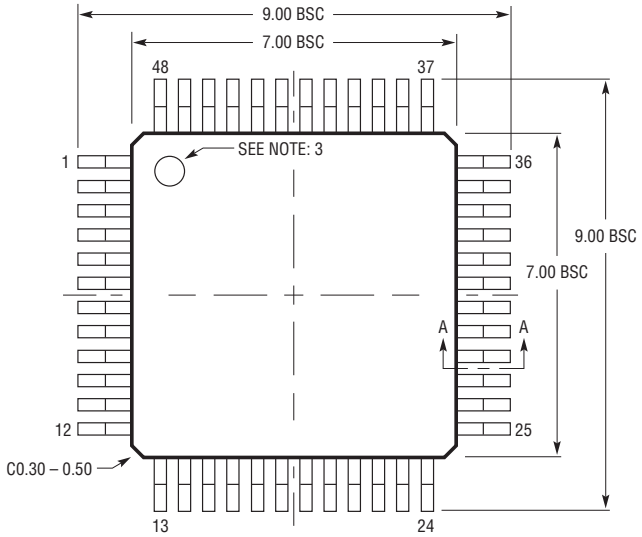
NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WKKD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

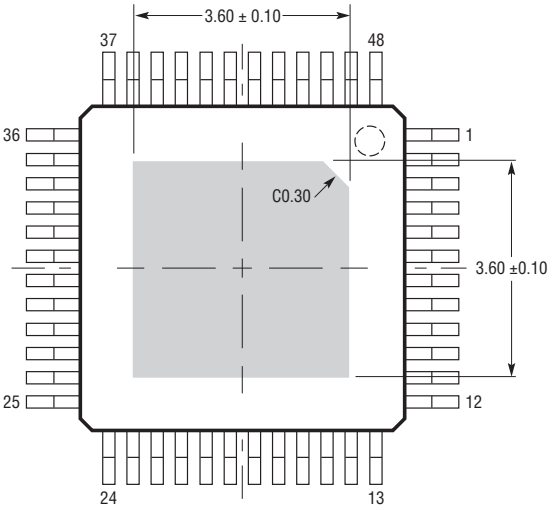
PACKAGE DESCRIPTION

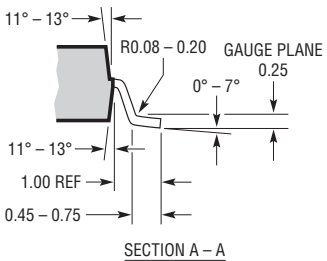
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

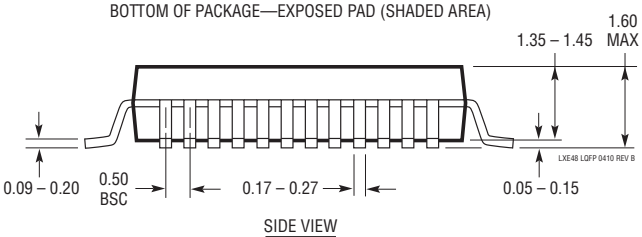
LXE Package
48-Lead Plastic Exposed Pad LQFP (7mm × 7mm)
(Reference LTC DWG # 05-08-1832 Rev B)







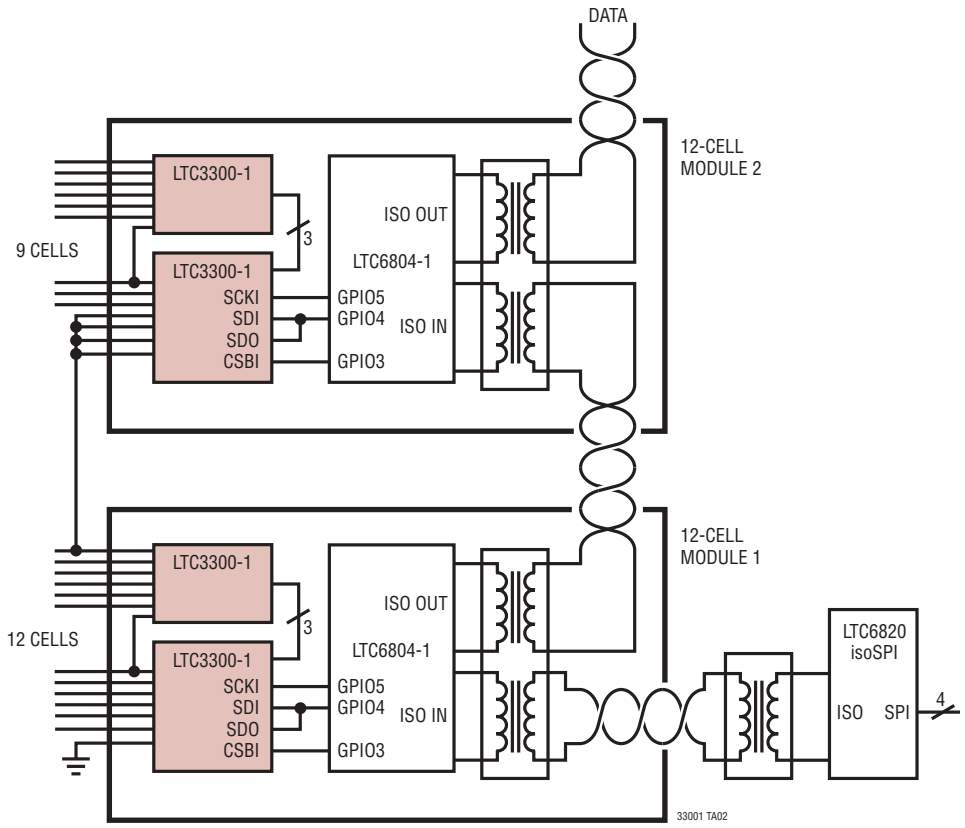




NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DIMENSIONS OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.25mm ON ANY SIDE, IF PRESENT
3. PIN-1 INDENTIFIER IS A MOLDED INDENTATION, 0.50mm DIAMETER
4. DRAWING IS NOT TO SCALE

TYPICAL APPLICATIONS

LTC3300-1/LTC6804-1 Serial Communication Connections



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC6801	Independent Multicell Battery Stack Monitor	Monitors Up to 12 Series-Connected Battery Cells for Undervoltage or Overvoltage, Companion to LTC6802, LTC6803 and LTC6804
LTC6802-1/LTC6802-2	Multicell Battery Stack Monitors	Measures Up to 12 Series-Connected Battery Cells, 1st Generation: Superseded by the LTC6803 and LTC6804 for New Designs
LTC6803-1/LTC6803-3 LTC6803-2/LTC6803-4	Multicell Battery Stack Monitors	Measures Up to 12 Series-Connected Battery Cells, 2nd Generation: Functionally Enhanced and Pin Compatible to the LTC6802
LTC6804-1/LTC6804-2	Multicell Battery Monitors	Measures Up to 12 Series-Connected Battery Cells, 3rd Generation: Higher Precision Than LTC6803 and Built-In isoSPI Interface
LTC6820	isoSPI Isolated Communications Interface	Provides an Isolated Interface for SPI Communication Up to 100m Using a Twisted Pair, Companion to the LTC6804

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