LINEAR TECHNOLOGY

DESIGN NOTES

# 16-Bit ADC Simplifies Current Measurements

Design Note 341

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## Introduction

The LTC®2433-1 is a high performance 16-bit Delta-Sigma ADC for DC measurements. With an input noise floor of 1.45$\mu V_{RMS}$ and a reference range of 100mV to $V_{CC}$, the input resolution and range can be optimized for a wide variety of applications. The flexible SPI interface can be configured to self-clock, simplifying isolation or level shifting of digital signals in applications where the ADC must be referenced to a different potential than the data acquisition system.

## Data Transfer

Figure 1a shows a –48V telecom supply current monitor with a 5.4A full scale. The LTC2433-1 serial interface is configured for internal serial clock, continuous conversion mode. This mode is selected by tying chip select low and pulling SCK high at power-up. In this mode, the LTC2433-1 continuously converts at 6.8 samples per second and clocks out its data at a serial data rate of 17.5kHz ±2%, the tolerance of the internal oscillator.

The LTC2433-1 serial data format lends itself to asynchronous reception. While a conversion is taking place, SDO is high. At the end of a conversion, SDO goes low for two clock cycles ($\overline{EOC}$ and DUMMY bits) and then continues outputting the remaining data bits. Thus the $\overline{EOC}$ bit can be used as a start bit as in standard asynchronous communication schemes such as RS232. Unfortunately, the internal oscillator tolerance makes it risky to receive all 19 bits asynchronously. One solution is to apply a crystal-controlled clock signal to the $F_O$ pin, but there is a simpler (and cheaper) way.

Exclusive ORing the SDO and SCK signals produces a serial data signal with embedded clock information similar to Manchester encoding that can easily be decoded by a microcontroller or FPGA. The data format is shown in Figure 2.

While a conversion is taking place, both SCK and SDO are high, so the XOR output is low. At the end of a conversion, both SDO and SCK fall, which may produce a glitch of up to 10ns as these edges are separated only by internal gate delays. The receiving device should look for a high level for at least 20ns to ensure that it is the start bit and not a glitch. (The optocoupler circuit shown does not respond to a pulse narrower than 500ns, so the glitch is not a problem.) The next rising edge is the center of the DUMMY bit, which synchronizes the sampling of the SIGN bit three quarters of one bit period later. After sampling SIGN, the



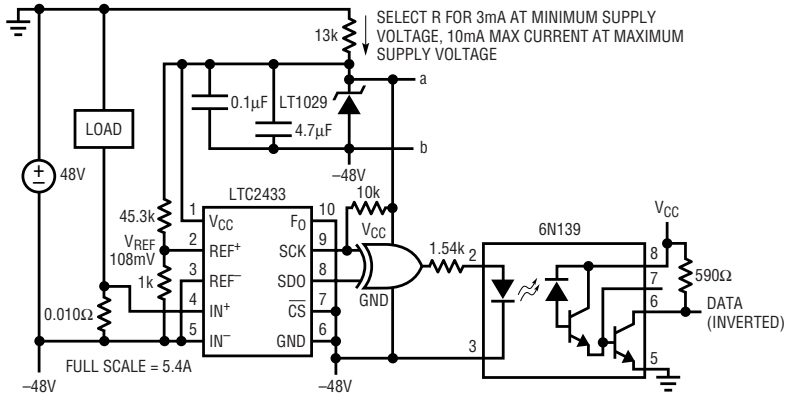
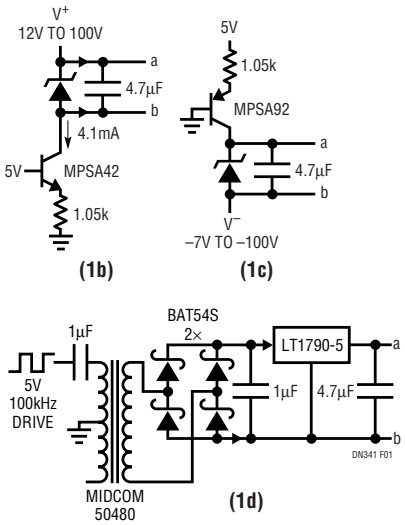



Figure 1a. –48V Current Monitor



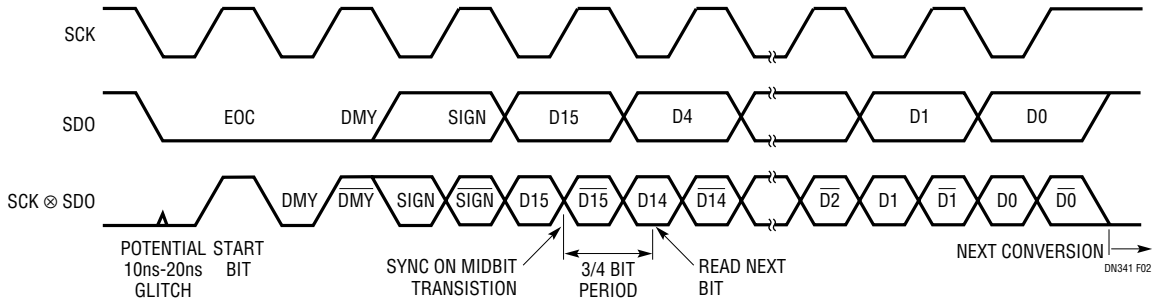



**Figure 2. Timing Diagram**

next transition starts another three-quarter bit period delay to synchronize the sampling of D15. The procedure continues until all data bits are received.

This data reception technique tolerates a total timing error of –50% to 33% including errors due to differences between the optocoupler rise and fall times, timing error of the receiving device and the 2% error of the LTC2433-1 internal oscillator.

## Data Reception Pseudocode

The following pseudocode can be ported to an appropriate microcontroller or used to design a state machine in a programmable logic device.

1. Wait for data high state for more than 20ns.
2. Wait for low. This is the end of the start bit.
3. Wait for transition (middle of dummy bit).
4. Wait three-quarters of a clock period.
5. Sample SIGN, wait for transition.
6. Wait three-quarters of a clock period.
7. Sample D15, wait for transition.
8. Wait three-quarters of a clock period.
9. Sample D14, wait for transition.
10. Continue until all bits are read.

The circuit was tested using a PIC microcontroller running at 20MHz. Code should be thoroughly tested for adequate timing margins. Also, good programming dictates that code should have timeouts in case an edge is missed, as might occur if the data reading procedure is pre-empted by an interrupt. This can be as simple as aborting a read if it takes more than double the theoretical time for all 19 bits to be clocked out.

## Power and Analog Inputs

Power and reference in Figure 1a are derived from an LT®1029 precision shunt reference. The series resistor should be chosen such that the LT1029 current is at least 1mA at all times. While a conversion is taking place, the LTC2433-1 draws 200μA. During the data output phase, ADC current drops to 4μA and the 6N139 optocoupler draws 2mA at 50% duty cycle. The 6N139 meets the low input current and medium speed requirements of this application. Data inversion is required to keep the LED off while a conversion is taking place.

The 5V reference is divided down to 108mV for current measurements, giving a differential input range of ±54mV to match standard 50mV output current shunts with 4mV of over range capacity. For voltage monitoring applications, the 5V reference can be used directly and the input can be divided to accommodate the resulting ±2.5V input range.

This circuit can be adapted to a wide variety of applications. Figure 1b is suitable for high side current sensing up to 100V (limited by dissipation in the current source transistor). Figure 1c is for low side sensing of negative supplies. Figure 1d is a fully isolated supply using a small telecom transformer and an LT1790-5 series reference for both power and reference voltage.

## Conclusion

The LTC2433-1 is a simple and cost effective solution to challenging DC monitoring problems. It is possible to simplify applications that once required complex (and inaccurate) analog level shifting by placing this highly accurate ADC “at the source”—all that is needed is a creative, but simple use of the differential input and reference, along with the flexible SPI interface offered by the LTC2433-1.

**Data Sheet Download**

http://www.linear.com/go/dnLTC2433

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