LINEAR TECHNOLOGY
DESIGN NOTES

“Easy Drive” Delta-Sigma Analog-to-Digital Converters Cancel Input Current Errors – Design Note 368

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Introduction

It is now possible to place large RC networks directly in front of high resolution ΔΣ analog-to-digital converters without degrading their DC accuracy (see Figure 1). The LTC®248x family of converters solves this problem with Easy Drive™ technology, a fully passive sampling network that automatically cancels the differential input current. Easy Drive technology does not use on-chip buffers, which compromise performance (see What is Wrong with On-Chip Buffers?), but instead uses a new architecture that maintains 0.002% full-scale error with input RC networks up to 100kΩ and 10μF. This new technology offers many advantages over previous generation ΔΣ ADCs:

- Rail-to-rail common mode input range
- Direct digitization of high impedance sensors
- Elimination of sampling spikes seen at the ADC input pins
- Simple external lowpass filtering
- Noise/power reduction
- Cancellation of external RC settling errors
- Easy interface to external amplifiers
- Removal of transmission line effects for remote sensors

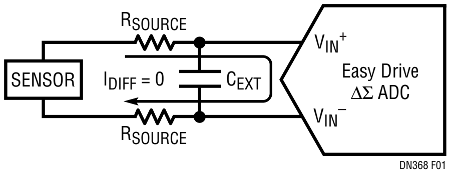

Figure 1. Easy Drive Technology Automatically Cancels Differential Input Current, Thus Allowing Direct Digitization of Large External RC Networks

How Does it Work?

Delta-Sigma converters achieve high resolution by combining many low resolution conversions into one high resolution result. Most commercially available ΔΣ converters combine hundreds or even thousands of 1-bit conversions into a single 16-, 20- or 24-bit result. The obvious advantage is that it’s much easier to implement a 1-bit converter than a 24-bit converter. In order to achieve high resolution, the input is sampled many times during the conversion cycle.

The problem is that the input structure of ΔΣ converters is a switched capacitor network. Capacitors are rapidly switched (up to 10MHz) between the input, reference and ground as a function of the final output code. Each time these capacitors are switched to the ADC input, a current pulse is generated. A pattern of charging/discharging pulses is seen at the input pin of the ADC. This pattern is a complex function of the input and reference voltages. External RC networks that do not completely settle during each sample period cause large DC errors.

The trick to solving this problem is to take advantage of the oversampling properties of ΔΣ converters. The front-end capacitor switching on a per sample basis is identical to conventional ΔΣ converter sampling. An innovative front-end sampling architecture controls the switching pattern of the capacitor array. When summed over the entire conversion cycle, the total differential input current is zero, independent of the differential input voltage, common mode input voltage, reference voltage or output code. The common mode input current is constant and proportional to the difference between the input common mode voltage and reference common mode voltage.

RC networks placed in front of ΔΣ ADCs significantly improve their performance and ease-of-use while providing lowpass and antialias filtering. External RC networks applied to the input of the LTC248x simply integrate (average) the input current spikes generated by the ADC. Since the average differential input current is zero, the total error introduced by the external RC network is zero if the resistance tied to the plus/minus inputs of the ADC is balanced. Resistances up to 100k, combined with

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capacitors up to 10µF may be placed in front of the ADC with less then 0.002% full-scale error (20ppm), while conventional $\Delta\Sigma$ ADCs with the same input network have greater than 10% full-scale errors (100,000ppm). Furthermore, no errors are introduced even if the external resistances are not balanced, as long as the common mode input voltage is equal to the common mode reference voltage. Even if the common mode input voltage does not match the common mode reference voltage, the differential input current remains zero and the common mode input current results in an offset voltage which may be removed through system calibration.

Direct digitization of external sensors with impedances up to 100kΩ is now possible without the need for external or on-chip amplifiers (see Figure 2). Bridges, RTDs, thermocouples and other sensors may tie directly to the ADC input. The addition of external capacitors reduces the charge kickback spikes seen at the input of the ADC. An external 1µF capacitor reduces a 1V spike to 18µV. This improves the noise performance of systems where the sensor cannot be placed near the ADC input and eases the drive requirements in applications where external amplifiers are used. The addition of a large resistor between the amplifier output and the ADC input isolates the amplifier from the large bypass capacitor, thus improving its stability.

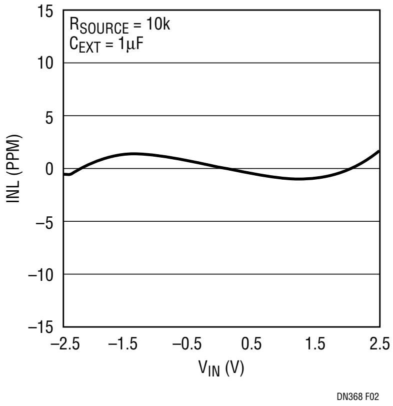

Figure 2. Easy Drive Technology Directly Digitizes Large External RC Networks Without Degrading Linearity

What is Wrong with On-Chip Buffers?

One historical solution to the input current settling problem is to integrate a buffer amplifier on the same chip as the $\Delta\Sigma$ ADC. This isolates the ADC input from the switched capacitor array making the ADC input appear high impedance. While this solution looks good on paper, the fact is data converters using on-chip buffers suffer from the limitations of those amplifiers. The common mode input range can no longer swing rail-to-rail. Input signals need to be shifted at least 50mV above ground and a volt or more below V_{CC}. Amplifier offset errors, offset drift, PSRR, CMRR and noise are combined directly with the input signal and result in reduced converter performance. Additionally, on-chip amplifiers require significant power in order to drive the high speed capacitive sampling network. For these reasons, most manufacturers of $\Delta\Sigma$ ADCs using this technology offer a mode to shut off and bypass on-chip amplifiers.

Another solution is coarse/fine input sampling. During the first half of the sampling period (coarse), the input voltage is sampled through an on-chip buffer amplifier, thus isolating the ADC input from the charging capacitor. During the second half of the sampling period (fine), the buffer is switched off and the capacitor is tied directly to the input. While this decreases the magnitude of the spikes seen at the input of the ADC, it results in nonlinear settling errors as a function of op amp offset voltage, CMRR, input signal level and external RC time constants. For these reasons, manufacturer's of $\Delta\Sigma$ ADCs using this technology bypass coarse/fine sampling for input signal levels below 100mV.

Conclusion

New Easy Drive technology simplifies the drive requirements of $\Delta\Sigma$ ADCs. The solution lies in a purely passive input current cancellation algorithm that enables rail-to-rail inputs without the added power requirements of on-chip buffer amplifiers and the errors they introduce. Easy Drive technology enables $\Delta\Sigma$ ADCs to directly interface to high impedance sensors, lowpass filters and input bypass capacitors without degrading the DC performance.

Devices using the Easy Drive technology are currently available in 16- and 24-bit versions with an on-chip temperature sensor, no latency conversions for simple multiplexing, on-chip oscillators with guaranteed line frequency rejection, precise DC specifications and the ease-of-use common to all of Linear's $\Delta\Sigma$ ADC converters.

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